KAUTILYA
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PUBLIC POLICY

CAPSTONE PROJECT

The Semiconductors Race– Understanding the challenges in India's technology and industrial ecosystem, and learning from global strategies

Capstone Project Number: CP-2026-07

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Cite this Report *as RK, H.N (2026). The Semiconductors Race– Understanding the challenges in India's technology and industrial ecosystem, and learning from global strategies. Available at: https://kspp.edu.in//capstone-project/the--semiconductors-race–understanding-the-challenges-in-india's-technology-and-industrial-ecosystem-and-learning-from-global-strategies*

The Semiconductors Race – Understanding the challenges in India's technology and industrial ecosystem, and learning from global strategies

Submitted to Kautilya School of Public Policy in Partial Fulfillment of the Requirement for the Degree of Master of Public Policy (MPP) 2024-26

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SELF-DECLARATION

This is to certify that the thesis titled "The Semiconductors Race – Understanding the challenges in India's technology and industrial ecosystem, and learning from global strategies" is my original work and has not previously formed the basis for the award of any Degree, Diploma, Associateship or Fellowship to this or any other University.

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This is to certify that the thesis titled **"The Semiconductors Race– Understanding the challenges in India's technology and industrial ecosystem, and learning from global strategies"** is original work undertaken by Harish Nandha RK, under my supervision and guidance as part of his Master's degree in this Institute. The thesis may be sent for evaluation.

Kanica

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ACKNOWLEDGMENTS

The author would like to express sincere gratitude to Dr Kanica Rakhra for her guidance, critical feedback, and intellectual support throughout the course of this study. The author would also like to thank Kautilya School of Public Policy for providing the academic environment and resources that made this research possible. This study has benefited greatly from the publicly available work of researchers, think tanks, and policy institutions whose scholarship forms the foundation of this analysis. Any errors or omissions remain solely the responsibility of the author.

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GLOSSARY

Abbreviation	Full Form
ADAS	Advanced Driver Assistance Systems
AICTE	All India Council for Technical Education
AI	Artificial Intelligence
ALD	Atomic Layer Deposition
ASIC	Application Specific Integrated Circuit
ASML	Advanced Semiconductor Materials Lithography
ATMP	Assembly, Testing, Marking and Packaging
AWS	Amazon Web Services
CapEx	Capital Expenditure
C-DAC	Centre for Development of Advanced Computing
CMP	Chemical Mechanical Planarization
CoWoS	Chip-on-Wafer-on-Substrate
CPU	Central Processing Unit
CVD	Chemical Vapor Deposition
DLI	Design Linked Incentive
DRAM	Dynamic Random Access Memory

DUV	Deep Ultraviolet Lithography
ECU	Engine Control Unit
ECMS	Electronics Components Manufacturing Scheme
EDA	Electronic Design Automation
EMC	Electronics Manufacturing Clusters
EUV	Extreme Ultraviolet Lithography
EV	Electric Vehicle
FDPR	Foreign Direct Product Rule
FDI	Foreign Direct Investment
GCC	Global Capability Center
GDP	Gross Domestic Product
GERD	Gross Expenditure on Research and Development
GPU	Graphics Processing Unit
GW	Gigawatt
HPC	High Performance Computing
HVAC	Heating, Ventilation and Air Conditioning
IC	Integrated Circuit

ICT	Information and Communications Technology
iCET	Initiative on Critical and Emerging Technologies
IDM	Integrated Device Manufacturer
IMEC	Interuniversity Microelectronics Centre
IoT	Internet of Things
IP	Intellectual Property
IPEF	Indo-Pacific Economic Framework
ISM	India Semiconductor Mission
ITIF	Information Technology and Innovation Foundation
ITSI	International Technology Security and Innovation
LED	Light Emitting Diode
MCU	Microcontroller Unit
MEMS	Micro-Electro-Mechanical Systems
METI	Ministry of Economy, Trade and Industry (Japan)
MITI	Ministry of International Trade and Industry (Japan)
MoC	Memorandum of Cooperation
MoU	Memorandum of Understanding

MSME	Micro, Small and Medium Enterprises
NAND	Not And (Flash Memory)
NIELIT	National Institute of Electronics and Information Technology
NOR	Not Or (Flash Memory)
OECD	Organisation for Economic Co-operation and Development
OEM	Original Equipment Manufacturer
OSD	Optoelectronics, Sensors and Discretes
OSAT	Outsourced Semiconductor Assembly and Test
PDK	Process Design Kit
PLI	Production Linked Incentive
PMIC	Power Management Integrated Circuit
PPP	Purchasing Power Parity
PSMC	Powerchip Semiconductor Manufacturing Corporation
PVD	Physical Vapor Deposition
R&D	Research and Development
SIA	Semiconductor Industry Association
SiP	System-in-Package

SMART	Skilled Manpower Advanced Research and Training
SME	Semiconductor Manufacturing Equipment
SRAM	Static Random Access Memory
STEM	Science, Technology, Engineering and Mathematics
STI	Science, Technology and Innovation
TPU	Tensor Processing Unit
TRUST	Transforming the Relationship Utilizing Strategic Technology (USA)
TSMC	Taiwan Semiconductor Manufacturing Company
UPW	Ultrapure Water
VCU	Vehicle Control Unit
VLSI	Very Large Scale Integration
WIPO	World Intellectual Property Organization
WSTS	World Semiconductor Trade Statistics

EXECUTIVE SUMMARY

Semiconductors have transitioned from a technological input to a strategic asset, underpinning economic competitiveness and national security. The COVID-19 pandemic exposed the vulnerabilities of a geographically concentrated global semiconductor supply chain, accelerating the "semiconductors race" worldwide. India has also launched its own policy architecture through the India Semiconductor Mission.

This study argues that the semiconductor industry is shaped by three mutually reinforcing forces – Technology, Industry, and Geopolitics – and that national semiconductor strategies succeed or fail depending on whether these three pillars are mutually interacting with each other. Drawing on the historical trajectories of countries that have fared strongly in the semiconductor industry, this study uses the three-pillar framework and applies it as a diagnostic tool to evaluate India's semiconductor ambitions.

Applied to India, the diagnostic reveals structural weaknesses across all three pillars. India's R&D spending at 0.7% of GDP, less private sector participation in R&D, weak industry-academia linkages, and a projected shortfall of 2.5 to 3 lakh semiconductor professionals by 2027 point to a fragile technology pillar. India's electronics manufacturing base, despite its recent growth, remains in low-value assembly with domestic value addition as low as 15-20%, and infrastructure bottlenecks in power, water, and land constrain its industrial pillar. And while India has built a significant diplomatic architecture through the TRUST initiative, Quad, Pax Silica, and bilateral agreements with Taiwan, Japan, and Singapore, the technology being transferred is limited to mature nodes, and India's ties with Russia create a credibility gap that limits deeper integration into the US-led semiconductor alliance network.

This study recommends a sequenced approach for India: Prioritizing ATMP and design in the short term, expanding the downstream industrial base and reforming the R&D ecosystem in the medium term, and aligning fabrication expansion with ecosystem maturity in the long term.

Keywords: *Semiconductors, Global Value Chain, Techno-Industrial Policy, Geopolitics, Technology Transfer, Industrial Ecosystems, India Semiconductor Mission*

1. Introduction

Enabling the storage, processing, and transmission of information across a wide range of modern technologies – from consumer electronics and telecommunications to artificial intelligence and advanced defense systems, semiconductors have become the critical infrastructure the modern digital economy relies on. As many aspects of today's economic activity, governance systems and military capabilities become increasingly dependent on digital systems, semiconductors have transitioned from being a technological input to becoming a strategic asset, central to both economic competitiveness and national security.

The global discourse surrounding semiconductors has intensified in recent years due to a convergence of structural and geopolitical factors. The COVID-19 pandemic exposed the vulnerability in the global supply chains, particularly in industries that are dependent on highly specialized yet geographically concentrated production hubs. Sudden shifts in demand – such as the surge in consumer electronics alongside fluctuations in the automobile sector – led to widespread chip shortages, revealing the systemic risks associated with overdependence on a limited set of production hubs. These vulnerabilities were especially pronounced due to the high concentration of semiconductor manufacturing capacity in East and Southeast Asia.

The rapid expansion of artificial intelligence, digitization of economies, transition toward renewable energy systems, and the growth of electric mobility have all driven sustained demand for mature technology chips, as well as advanced and specialized chips. Concurrently, rising geopolitical tensions and the increasing technological intensity of modern warfare have reinforced the role of semiconductors as critical components of national security. In this context, access to semiconductor supply is being seen through the lens of resilience, control, and technological sovereignty. As a result, States across the world are actively intervening to secure their positions within the semiconductor ecosystem, giving rise to the "Silicon Nationalism" phenomena (Zhou, 2022).

However, the semiconductor industry presents a unique challenge for such state ambitions. It is a highly fragmented and specialized global value chain, comprising distinct segments. Each segment is characterized by different technological requirements, capital intensities, and entry barriers. Moreover, the industry is marked by compounding innovation dynamics, where leading firms sustain their advantage through continuous reinvestment in research and development, making it difficult for late entrants to catch up. Consequently, no single country or firm today exercises dominance across the entire value chain; instead, leadership is distributed across highly specialized actors.

This structural complexity raises a critical policy question: how can late entrants strategically position themselves within the global semiconductor ecosystem? Much of the current policy discourse, particularly in emerging economies, is driven by the ambition to develop end-to-end semiconductor capabilities, including advanced fabrication facilities. Yet, the historical experience of leading semiconductor nations suggests that successful entry into this industry has been selective, sequenced, and closely aligned with domestic capabilities, institutional structures, and geopolitical context.

For India, this question is particularly salient. As a rapidly digitizing economy with growing ambitions in electronics manufacturing, artificial intelligence and defense, access to reliable semiconductor supply is essential for sustaining economic growth and ensuring strategic autonomy. At the same time, India remains largely absent from critical segments of the semiconductor value chain, especially in fabrication and upstream segments. However, given the capital intensity, technological complexity, and ecosystem requirements of the industry, the viability of a full-spectrum approach remains uncertain.

This study argues that the semiconductor industry should be understood as a globally fragmented yet specialized value chain with segment-specific barriers to entry, and that national strategies must be aligned accordingly. Rather than pursuing segment agnostic self-sufficiency, countries have historically succeeded by specializing in specific segments, leveraging state support, integrating into global supply chains, and building capabilities over time. Building on this, this study also argues that the semiconductor industry is highly influenced by geopolitical and geoeconomic factors, and countries building their individual industrial and innovation capabilities are capable of sustaining their semiconductor industries, thus making them resilient to international events. Drawing on an analysis of the semiconductor value chain and the techno-industrial trajectories of leading countries, this study examines the strategic options available to India and proposes a sequenced approach to entering and scaling within the semiconductor ecosystem.

2. Types of semiconductor devices and their applications

The classification of semiconductors can be done based on various factors. Their definitions can also vary according to various factors. But, for the ease of understanding of their technicalities and for the ease of understanding from a policy perspective, this paper combines classifications from OECD, World Semiconductor Trade Statistics (WSTS), Semiconductor Industry Association (SIA) and major private players. Based on this understanding, semiconductor chips can be broadly classified into five categories, namely:

1. Logic
2. Memory
3. Analog
4. Optoelectronics, Sensors and Discretes (OSD)
5. Others

1.1 Logic chips

Logic chips act as the “brain” of the electronic device and help the device perform calculations and operations by processing binary information. These chips are what make up the Central Processing Units (CPUs), Graphics Processing Units (GPUs), Tensor Processing Units (TPUs), etc. In the case of logic chips, the smaller the transistor, the faster is the flow of information. At the same time, increasing the number of transistors per chip allows the chip to perform a higher number of calculations, thus enabling it to give much better outputs. Thus, engineers have been finding ways to reduce the size of each transistor while trying to increase the number of transistors per chip. It is in this context that the size of the transistor is used to denote the performance capacity of the chip, as in 5nm chip, 3nm chip, etc. The latest most advanced chip consists of transistors of 3nm node size. The challenge engineers face is to keep up with the rising costs of packing an enormously increasing number of transistors while reducing their size (Organisation for Economic Co-operation and Development, 2024; Vempati et al., 2024). Logic chips are used in almost all electronic devices such as smartphones, laptops, computers, data centers, AI systems, EVs, etc.

1.2 Memory chips

Memory chips, as the name suggests, store data. They are further classified into two – Volatile memory chips, which lose the data when power is turned off; and Non-volatile memory chips which store data even when power is turned off. Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) are volatile memory technologies, storing data only temporarily, while Flash memory is the most common type of non-volatile memory chip technology. Not And (NAND) and Not Or (NOR) are the two main types of Flash memory, out of which NAND Flash is the most widely used and highly commercialized one for data storage purposes.

As the need for faster access and storage of data is evolving, the need to move beyond traditional ways of storing data is needed owing to the limitations they pose. 3D stacking of multiple memory cells using mature nodes is one latest advancement of memory storage. The latest advancement shows that flash memory chips are packing around 200 memory cell layers, and this technology is forecasted to reach upto 1000 layers by 2030. Apart from these, novel magnetic based, ferroelectric based and macromolecular based are newly evolving technologies to store data electronically. Memory storage primarily uses nodes ranging between 10nm and 50nm size (Organisation for Economic Co-operation and Development, 2024; Vempati et al., 2024).

1.3 Analog chips

Analog chips are used to work with analog signals, opposite to what digital chips do – digital chips are designed to work with and process digital signals. Analog chips are important because around 90% of real world signals are analog in nature (such as sound, temperature, etc.), and not digital. This means that the interface between digital electronics and the real world is achieved with the help of analog chips. These chips help in power management and power regulation, signal conversion and signal processing, signal amplification, etc. Analog chips work in conjunction with sensors and transducers which have become more and more important in today's era of automation, IoT, machine-to-machine communication, etc. (Dimension Market Research, 2025; Ivana & Ivana, 2025; Kerstin, 2024).

Analog chips are important for:

IoT, sensors, and edge devices: Sensor front-ends – for example, temperature monitors, humidity monitors, light monitors, pressure monitors, door locks monitors, etc. These have direct applications in modern "smart devices" such as thermostats, smart meters, security cameras, occupancy sensors, door sensors, etc.

Automotives applications: These chips help in power management, battery monitoring, battery health monitoring, sensor signal processing, helping advanced driver-assistance systems (ADAS), better control of electric motors, Engine Control Units (ECUs) and Vehicle Control Units (VCUs), EV battery chargers, consumer AC/DC adapters, in-vehicle infotainment systems, etc.

Consumer electronics: These chips help manage audio, display, power functions in electronics such as smartphones, laptops, wearables and other consumer durables such as refrigerators, washing machines, TVs, etc.

Industrial applications: They support robotics, machine vision (Image-sensor interfaces), predictive maintenance systems, industrial automation (machine-to-machine communication), etc.

Communication networks: They play a key role in base stations, network equipment, signal transmission systems, wireless communication, satellite communications.

Aerospace and Defence applications: They play a key role in remote operations, radar, guidance systems, avionics, precision control systems, etc.

Renewable Energy applications: They play a crucial role in power conversion, voltage regulation, energy storage systems, wind turbine converters, smart-grid meters, solar inverters, etc.

Healthcare and biomedical applications: With the rise in telemedicine and wearable health trackers, there is increased demand for patient monitors, imaging systems, hearing aids, and portable diagnostic tools. These chips play an important role in these applications.

1.4 Optoelectronics, Sensors & Actuators and Discretes (OSD)

Optoelectronics are semiconductor devices used to convert light into electricity and vice-versa. This includes light emitting diodes (LEDs), lamps, displays, lasers, image sensors, etc. Sensors and Actuators are semiconductor devices which are designed to show changes in the flow of electric current through them corresponding to changes in physical, chemical or biological properties such as temperature, pressure, displacement, velocity, acceleration, stress, strain, etc. Discretes refers to the basic building blocks of integrated circuits and other devices. They are basically single-function devices. Discretes include transistors (CMOS, MOSFET, BJT, etc.), diodes, thyristors, etc (WSTS, Inc., 2020).

These OSDs find applications in almost every modern device. Optoelectronics are extensively used in image sensors, which are used in phones, cameras – for automotive, surveillance and other purposes, printers, color sensors (RGB), ultraviolet sensors, fiber optic cables, diagnostic imaging, photovoltaic cells, infrared cameras, etc. Sensors and actuators are extensively used in places for monitoring physical/chemical/biological changes such as temperature (automatic temperature control, for example), pressure (tyre pressure monitoring system in automotives, for example), heart rate monitoring, motion sensing such as accelerometers and gyroscopes, which are used in mobile phones, drones, ADAS, etc. Discretes make up the building blocks of integrated circuits, and thus chips (Unisystem, 2024; WSTS, Inc., 2020).

2. Market share of the various categories of semiconductors

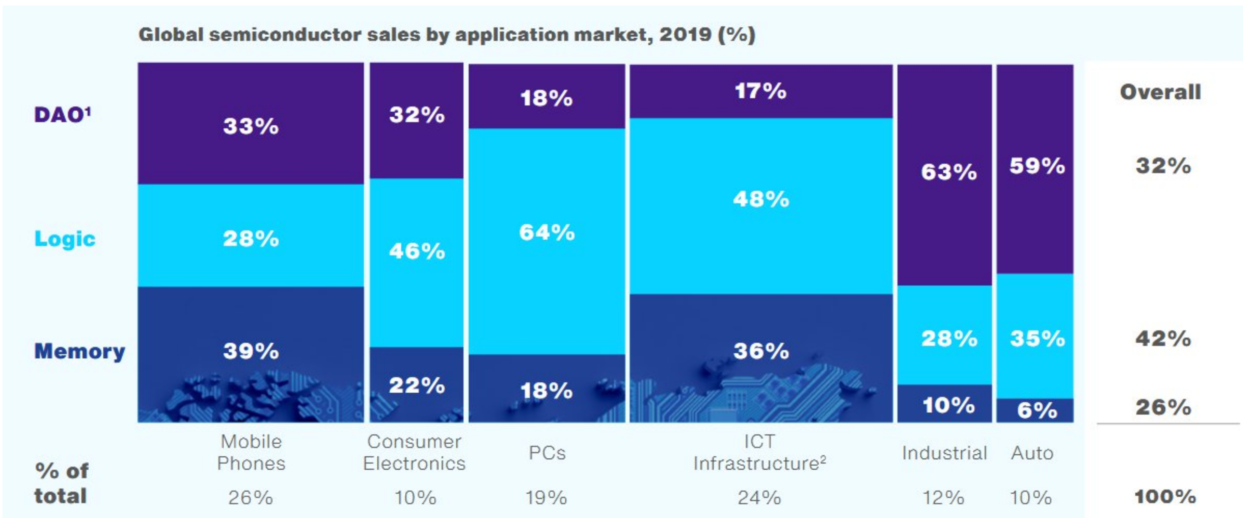

Figure 1 Global Semiconductor sales by application market, 2019 (%)

(Source: BCG analysis)

Logic chips dominate the market share of these categories, followed by DAO and then Memory. The demand for DAO chips can be attributed to their increased demand in the automotive segment, renewable energy segment and consumer electronics segment. It is worth noting here that all sectors of industry that need semiconductor chips need various types of chips for their overall functioning. There is no sector that can say it needs only one type of chip.

Out of the market consumption, mobile phones and ICT infrastructure consume the highest percentage of chips. Mobile phones consume more memory chips, followed by DAO and logic chips. Given the fact that mobile phone companies have started offering higher storage and in-device processing capabilities (the 8 GB RAM 128 GB storage variant often seen in advertisements is an example) and since mobile phones also use a lot of discrete components, displays and sensors such as gyroscope, accelerometers, etc. in them, they also consume a huge amount of DAO chips.

The ICT infrastructure here majorly includes data centers,cloud computing service providers and telecom sector equipment (such as telecom towers). The rise in cloud computing services (such as Microsoft Azure and Amazon Web Services (AWS)) and the increased penetration of internet connectivity can be attributed to the ICT infrastructure segment consuming a huge chunk of semiconductor devices. ICT Infrastructure majorly consumes logic chips, since these hardware devices house large amounts of processing capabilities, catering to the increasing High-Performance Computing (HPC) demand and Application Specific Integrated Circuits (ASICs) for enabling HPC capabilities. Apart from GPUs and AI Accelerators, CPUs specifically made for these high-performance demanding applications have also been manufactured. NVIDIA dominates the GPUs market while AMD and Intel are leaders in the CPUs market.

A similar trend can be seen in case of semiconductor consumption in the PCs segment as well. Due to the growing needs for edge computing power, logic chips dominate the PCs segment as well. Industrial and Automotive segments consume more DAOs (the analog chips) because they deploy more analog chips and sensors in Energy Management Systems, Power Management Systems, Engine Control Units, industrial automation purposes, etc.

3. Process of manufacturing semiconductors and the global value chain

The entire semiconductor manufacturing process is often described as a complex multi-stage manufacturing process and involves approximately 500 discrete steps and takes four to six months for the entire process, from design to final packaging and distribution to be complete.

However, from an economic and policy perspective, this complexity is best understood not in terms of individual processes, but as a segmented global value chain, comprising distinct stages with different cost structures, capabilities, and entry barriers.

The entire process of manufacturing of semiconductors can be broadly divided into three categories:

1. Design
2. Fabrication
3. Assembly, Testing, Marking and Packaging (ATMP)

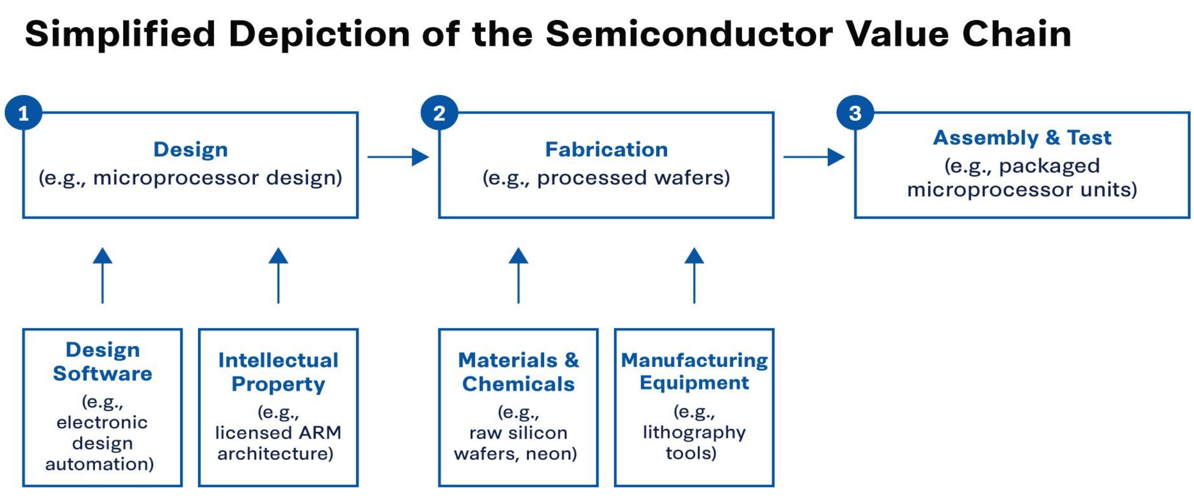

Figure 2 Process of manufacturing semiconductors

(Source: CSIS)

3.1 Design

The design of the chip plays the fundamental role in deciding how efficient and powerful the chip is going to perform. It involves the process of electronically designing the circuit to be manufactured (say, the number of transistors, the type of transistors, the size of transistors, etc.) for the specific process involved. This Design segment relies on three important inputs, namely:

1. Electronic Design Automation (EDA) tools: Chip Engineers use advanced EDA tools to design circuits, simulate performance, check for errors and prepare layouts for chip fabrication, optimizing for the chips' performance, cost and power. Major EDA providers are Cadence, Synopsys, and Siemens EDA.
2. Intellectual Property (IP) Cores: These are the existing core designs developed by chip manufacturers and core architecture leaders, which are licensed to design companies for further use. Major companies that license IP cores are ARM Holdings, Synopsys Inc., Cadence Design Systems, CEVA Inc., Rambus Inc.
3. Process Design Kits (PDKs): PDKs are used to ensure that the chip designs align well with the capabilities of the foundry. These PDKs are developed by foundries for their process nodes that contain the design rules of a node.

3.1.1 Key Characteristics of the Design Segment

The design segment is characterized by high R&D intensity, low physical capital requirements, and high value capture.

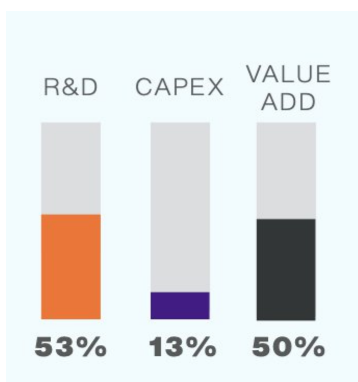

Figure 3 Key Characteristics of Design segment

(Source: BCG Analysis)

3.1.1.2 R&D Intensive

The design segment is highly R&D intensive, owing to the highly specialized and multi-year expertise in creating complex, efficient and high-performance chips. The chip design process involves more than 40 complex steps, and the cost of designing a chip varies widely depending on the feature size of the process node to be designed, the complexity of the circuit design, and the license costs associated with EDA tools and IP cores (OECD, 2025). For example, the costs associated with designing an advanced 3nm chip ranges from around USD 500 million to more than USD 1.5 billion. The costs associated with designing mature chips are also quite high, ranging around USD 50 million for 28nm chips, USD 298 million for 7nm chips, and around USD 542 million for 5nm chips (Accenture, 2024).

3.1.1.3 Low Capital Expenditure

Despite these high design costs, the segment is relatively low in capital expenditure (CapEx) compared to fabrication. It requires limited investment in physical infrastructure, with a greater reliance on intangible assets such as software, algorithms, and human capital. This is reflected in the asset composition of the segment, where intangible assets dominate over tangible ones.

3.1.1.4 High value-adding

The design segment captures a disproportionately high share of value, accounting for roughly 50% of the total value added in the semiconductor value chain. This high value capture can be attributed to the central role of design in determining chip performance and differentiation, as well as the relatively low input and intermediate costs compared to manufacturing stages.

3.1.2 Factors deciding the location of Design segment

The location of design activities is primarily determined by availability of skilled human capital and strength of the innovation ecosystem, rather than proximity to manufacturing facilities.

The Design segment's location largely depends on the skilled workforce, especially trained in advanced STEM education streams such as Very Large Scale Integration (VLSI), electronics engineering, and computer architecture. A deeply embedded R&D ecosystem – that includes research institutions, industry networks, strong industry-academia linkage – enable the firms to advance faster in the design segment value-chain since advances in this technology are rapid and exponential. The cost of and access to utilities also play a key role in deciding their location. The need for utilities here is that a vast network of data centers, High Performance Computing (HPC), and strong internet connectivity are some critical capabilities for this segment.

The rising cost of design and the long lead times associated with R&D introduce significant financial risks, making the segment a high-risk, high-reward domain. For example, designing a 5nm chip costs about USD 540 million, while designing a 7nm chip costs around USD 300 million and designing a 10nm chip costs around USD 175 million. The same trend is seen in the increasing cost of constructing fabs for producing these smaller chips as well. The dynamic in both these segments is that the investment takes a certain amount of time to give returns (which is true in many businesses).

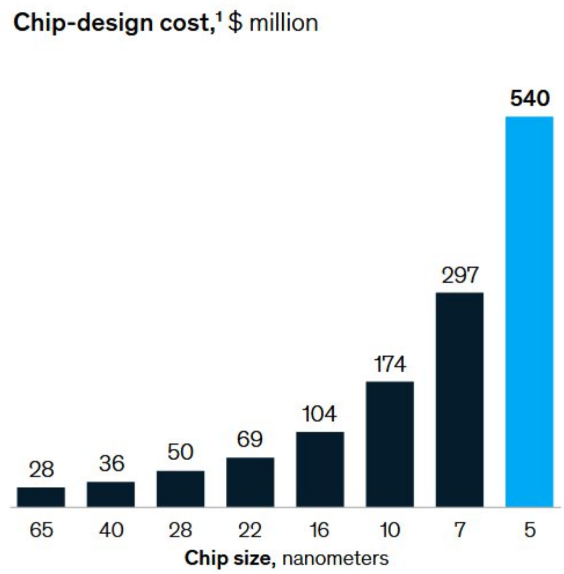

Figure 4 Chip design cost (in USD million)

(Source: McKinsey)

Unlike fabrication, the design segment does not depend heavily on physical infrastructure such as land, water, or energy. Instead, it thrives in environments that support knowledge creation, collaboration, and technological innovation.

3.1.3 Geographic Distribution of Design Segment

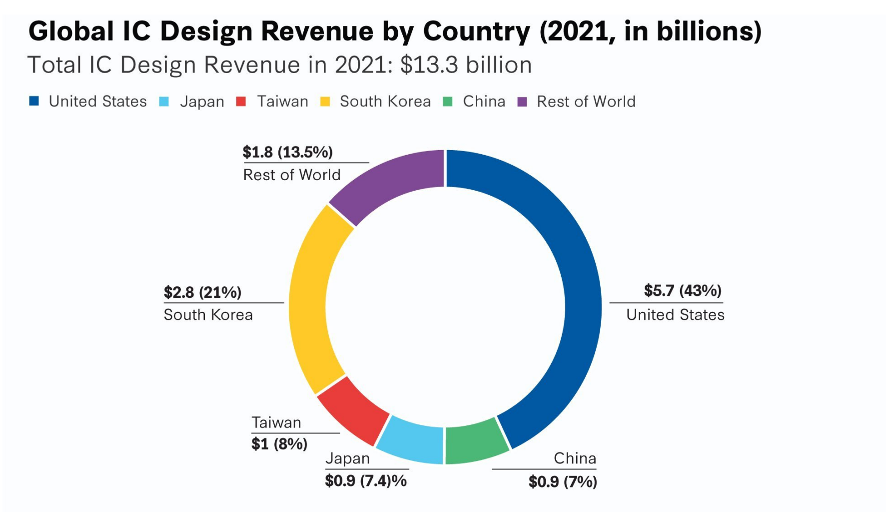

Figure 5 Global IC Design Revenue by Country (2021, in billions)

(Source: CSIS)

The design segment is highly concentrated geographically, with firms headquartered in the United States dominating the global market. US based companies account for approximately 43% of the global integrated circuit (IC) design market. In 2021, out of global IC design revenues of USD 13.3 billion, around USD 5.7 billion accrued to U.S. firms. South Korea follows with approximately 21% market share, while Japan and Taiwan and China hold smaller shares.

This dominance extends to key sub-segments. In the EDA market, three firms – Cadence Design Systems, Synopsys, and Siemens EDA – collectively control around 85% of the global market, with the United States accounting for approximately 96% of total market share. Similarly, the IP core segment is led by firms such as Arm Holdings, alongside US based companies, reinforcing the concentration of technological capabilities within a small number of countries (Broersma, 2025; Indian Council of World Affairs, 2024).

This geographic concentration reflects the importance of long-term investment in human capital, innovation ecosystems, and institutional support in shaping leadership within the design segment.

3.2 Fabrication

Once the design is finalized, the design is sent to a semiconductor fabrication plant (also called “fab”). Here, capital intensive and complex processes such as wafer fabrication, photolithography, deposition, etching, doping, implanting, planarization, passivation and other processes are used to build up and above 60 layers of transistors and other circuitry. Fabrication can be a complex 350 step process taking around 45 to 60 days for manufacturing mature nodes, or over 700 step process taking around 60 plus days for manufacturing advanced nodes (Accenture, 2024).

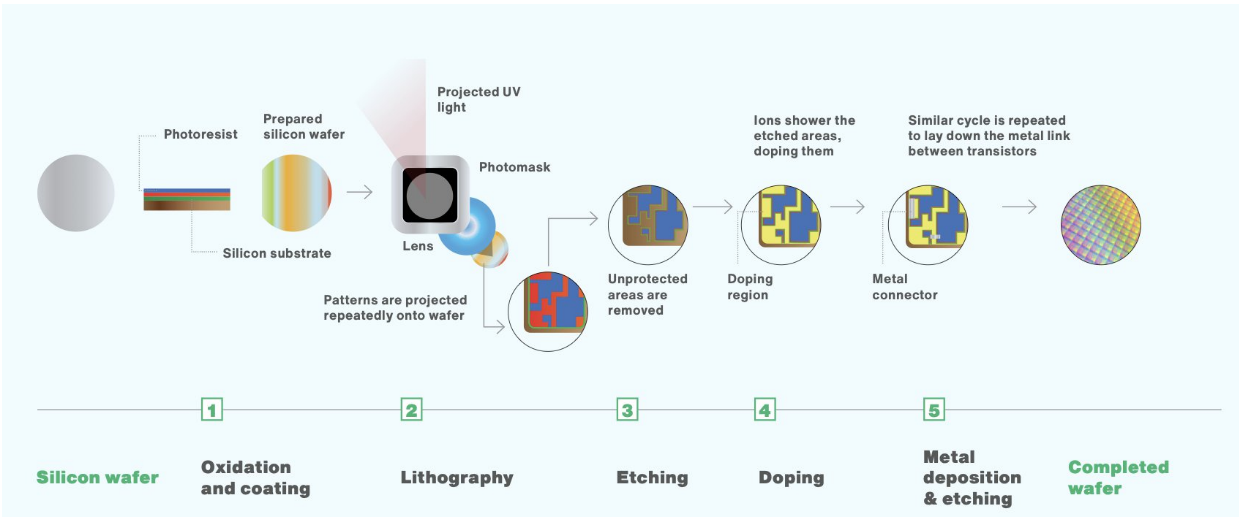

Figure 6 Fabrication process

(Source: BCG Analysis)

The semiconductor fabrication process can be broadly divided into the following:

1. *Silicon wafer fabrication*

This starts with the manufacturing of ultra-pure silicon wafers. Ultra-pure silicon wafers are manufactured using specific chemical processes (usually the Czochralski Pulling Method is used) to produce silicon blocks (called as ingots) from raw silicon. Then, specific diamond-coated blades are used to cut the silicon blocks into silicon wafers, usually 200mm and 300mm in diameter. The wafers are then cleaned, polished and made ready for further processes using specialty chemicals. (Bier, 2025; Varas et al., 2021; Branch Education, 2025; India Semiconductor Ecosystem Workforce Development Strategy Report 2025, 2025; Ray, 2025).

2. *Photolithography*

The next step is patterning – transferring the desired circuit design/pattern on the wafer. This process is called photolithography, where Ultraviolet Light is used to print the pattern onto the wafer. The latest technology in this photolithography is Extreme Ultraviolet Lithography (EUV), where UV light of wavelength 13nm is used. This advanced EUV technique is used to pattern the advanced chip circuit patterns – such as 7nm, 5nm, 3nm – while its predecessor technique, called Deep Ultraviolet Lithography (DUV), uses UV light of wavelength 193nm to pattern the circuits. EUV also uses highly precise and polished mirrors in the process while DUV uses lenses (Bier, 2025; Branch Education, 2025; Ray, 2025).

The ultra-pure silicon wafer is coated with a layer of photoresist – a light-sensitive chemical which undergoes certain chemical reactions on exposure to UV light that ends up patterning the desired circuit pattern on the silicon wafer. After the photoresist, the UV light is projected at the photomask which imprints the circuit design onto the UV light which then bounces off a set of mirrors (or lenses in case of DUV) in order to project a focussed and scaled down image of the mask onto the wafer. Wherever the UV light touches, the photoresist undergoes some chemical change and gets modified, thus imprinting the design onto the wafer (Bier, 2025; Branch Education, 2025; Ray, 2025).

3. *Etching, Deposition and Doping*

After photolithography, the photoresist chemical layer that remains unaltered is washed away by certain specialty chemicals or specialty gases. This process is called etching. Etching can be done in two ways – Wet Etching, which uses specialty chemicals to wash away the remaining layers of photoresist; and Dry Etching which uses specialty gases or plasma to wash away the remaining layers of photoresist.

After etching, doping process takes place. In this process, impurities such as Boron or Phosphorus or Arsenic are added to give the Silicon its semiconducting properties. Along with the doping process, deposition of metal ions such as Copper or Tungsten or any other metal takes place to "connect" the components of the chip. This step, called the Deposition step can be done using 3 methods:

1. Chemical Vapor Deposition (CVD)
2. Physical Vapor Deposition (PVD)
3. Atomic Layer Deposition (ALD)

Each of these processes use a variety of specialty chemicals or gases to perform their function. This process of patterning-etching-doping-deposition takes place repetitively in multiple cycles to print the desired number of component layers on the chip (Bier, 2025; Branch Education, 2025; Ray, 2025).

3.2.1 Key Characteristics of the Fabrication Segment

3.2.1.1 Extreme Capital Intensity

Semiconductor fabrication is a highly capital intensive process, contributed mainly by the following (Intel Newsroom, 2023; Varas et al., 2021):

1. Higher costs of fab construction
2. Higher costs of the specialised equipments used in the fabs
3. Higher costs of the special chemicals and gases used in the process of chips fabrication
4. Costs involved in upskilling of labour to keep up with the fast paced evolution of technologies – The presence of an already existing skilled workforce, trained in electronics, mechanical and allied engineering technologies is an added advantage

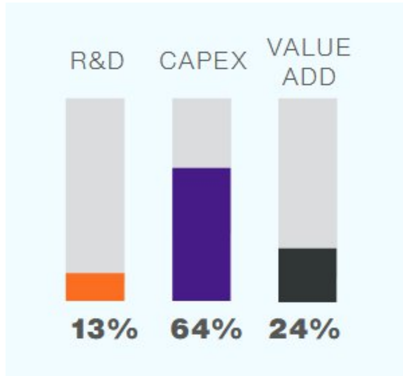

Figure 7 Key characteristics of Fabrication segment

(Source: BCG Analysis)

The CapEx required – including land, building, and equipment to construct a state-of-the-art fab ranges from USD 5 billion (for advanced analog fabs) to USD 20 billion (for advanced logic and memory fabs). The cost of constructing fabs is increasing as the size of the node is decreasing. Moreover, it takes three to five years to complete the construction and takes around 6000 construction workers to complete. A fab roughly houses around 1200 equipment worth millions of dollars and 1500 utility equipment. Another estimate shows that it would cost TSMC around USD 19.5 billion to construct its next 3nm fab. Besides being capital intensive, the successful operation of a fab requires deep knowledge of the complex process. These fabs also need ultra pure clean room environments with continuous supply of ultra pure water and undisrupted electricity (Intel Newsroom, 2023; Varas et al., 2021).

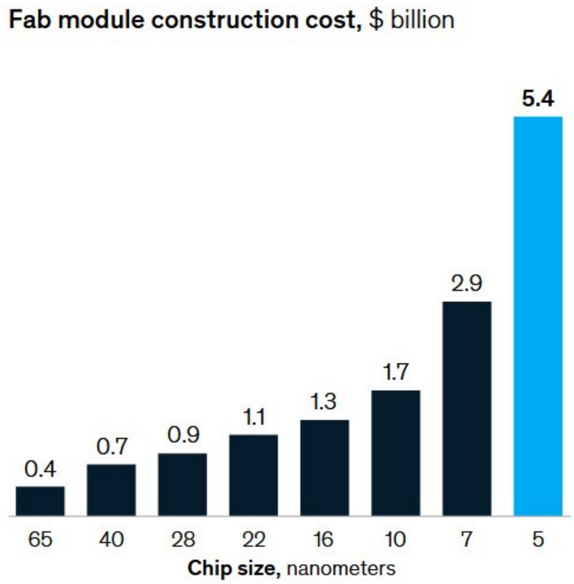

Figure 8 Fab construction cost (in USD billion)

(Source: McKinsey)

Despite accounting for a disproportionately high share of industry CapEx (around **64%**), fabrication contributes a relatively lower share of value-add (around 24%), reflecting its infrastructure-heavy nature.

The higher costs of building and running a fab has led to the evolution of four different business models for this semiconductor fabrication segment.

1. Integrated Device Manufacturers (IDMs): These firms design and fabricate the chips in their own facilities. These firms are the pioneers in the semiconductor industry. Examples of IDMs include Intel, Samsung, Texas Instruments.
2. Fabless Firms: These firms design the integrated circuits, and dedicate their resources for this service and outsource the manufacturing to pure-play foundries. Examples of Fabless firms are NVIDIA, Qualcomm, AMD, etc.

3. Pure-Play Foundries: These firms do not focus on chip design and dedicate their entire resources for the end-to-end fabrication business. A finest example of a pure-play foundry is the Taiwan Semiconductor Manufacturing Company (TSMC).
4. Outsourced Semiconductor Assembly and Test (OSAT) Firms: These firms specifically provide the ATMP services.

3.2.1.2 Economies of Scale and Utilization Dependence

The semiconductor fabrication process is highly scale-driven and it is important for fabs to operate with higher utilization rates and near full capacity. If the fabs operate at full capacity, they can start seeing profits in around five years. However, if their capacities are underutilized, the time it takes for the fabs to start seeing profits will increase, even with government support. For instance, if a fab is operated at around 50-55% capacity, even with government support of upto USD 2 billion it might take the fab 8 to 10 years to start seeing profits (Wiseman et al.,n.d.).

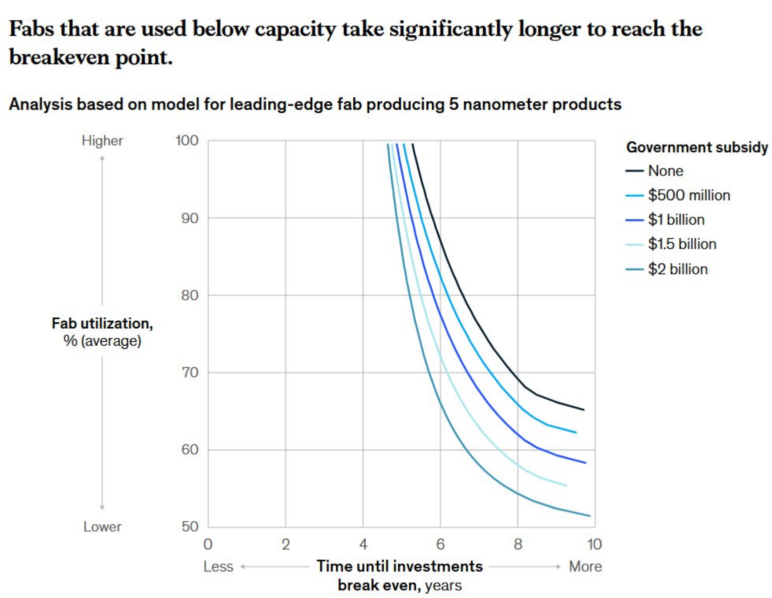

Figure 9 Fab utilization (%) vs time taken until investments break even (years)

(Source: McKinsey)

3.2.1.3 Resource and Infrastructure Intensity

Fabs require continuous and reliable access to critical utilities such as energy, water and cleanroom environments. Semiconductor fabs are energy intensive – for example, they consume around 4% of Taiwan's total energy usage. In 2021, the entire semiconductor industry consumed 149 billion kWh of electricity - enough to power a city of more than 2.5 crores population for a year. As chip technology sees advancements rapidly, more advanced chips will need more energy consumption at the fab level. This enormous continuous supply of electricity is important to power the large number of tools and equipment in the fabs, such as Ultrapure Water (UPW) plants, vacuum systems, HVAC systems – Heating, Ventilation and Air Conditioning systems. The UPW systems and waste water recycling and abatement systems themselves consume huge amounts of electricity. Grid electricity and fossil fuels constitute 95.8% of the total energy use, acting as the major sources of electricity that cater to this huge consumption industry while renewable energy accounted for only 2.7% (Ali, 2023; Blue Cape Economic Advisors, n.d.).

These fabs consume huge amounts of ultra-pure water. This UPW is required for cleaning, etching, deposition and other processes that ensure an ultra-pure clean environment for the further processes to occur. On an average, a fab consumes 2 to 10 million gallons of water per day. In 2021, major semiconductor companies around the world utilized approximately 789 million cubic meters of water, with primary sources being surface water (47%) and municipal supply (35.3%) (Ali, 2023; Blue Cape Economic Advisors, n.d.). Even minor disruptions in electricity or water supply can result in significant production losses.

These semiconductor fabs are huge. Each semiconductor fab is around 2.5 lakh square feet (each fab can house 4 American football fields in them, for instance), and thus require huge land parcels that are industrial grade. An additional point that leads to ready-to-use industrial land can be the reduced litigation complexities associated with property rights that often affect countries like India. Also, a land parcel to be certified as ready-to-use needs to have certain infrastructure facilities (Ali, 2023; Blue Cape Economic Advisors, n.d.), such as:

1. Easy access to roads / railways / airports – Transportation
2. Access to ports and logistics zones for easy import and export (since the semiconductor industry is highly globalized today)
3. Utility access at affordable rates – energy, water, etc.

Human resource – skilled and talented workforce – is of utmost importance for fabrication plants. Engineers, technicians and scientists from advanced STEM backgrounds are highly important. An already established related industrial base – for example, a strong electronics manufacturing industry – is a key deciding factor since it helps reduce the overall operational costs, enables skill and technology sharing and logistics costs sharing.

3.2.1.4 Dependence on Specialized Materials, Chemicals and Equipment Ecosystem

The semiconductor manufacturing process requires more than 100 key materials and chemicals needed as inputs. Specialty materials and chemicals are used in both front-end and back-end fabrication processes. The main front-end chemicals and materials include polysilicon, silicon wafers, photoresists and photomasks, high-performance polymers, CMP slurries, wet processing chemicals such as high-purity solvents, acids, etchants, strippers and gases used in doping, etching and deposition processes. The main back-end materials include leadframes, organic substrates, ceramic packages, encapsulation resins, bonding wires and die-attach materials, and dielectric coatings (Thadani & Allen, 2024; Varas et al., 2021).

Semiconductor manufacturing involves more than 50 different types of advanced wafer processing and testing equipment. Some of the major SME include Lithography tools, especially EUV and DUV machines. Apart from them, Metrology and Inspection equipment also hold a lot of value in the fabrication process since the entire fabrication process takes over 100 steps and one to two months to complete, and to ensure quality and defect-free process, adequate number of testing and quality control processes are kept at certain stages of the fabrication process. The fabs also use a lot of automation tools and process control systems, automated material transportation and real-time lot dispatching systems. Many new fabs are becoming fully automated as well. There are only a handful of firms that can manufacture these equipment, thus making their presence invaluable to the industry's value chain (Thadani & Allen, 2024; Varas et al., 2021).

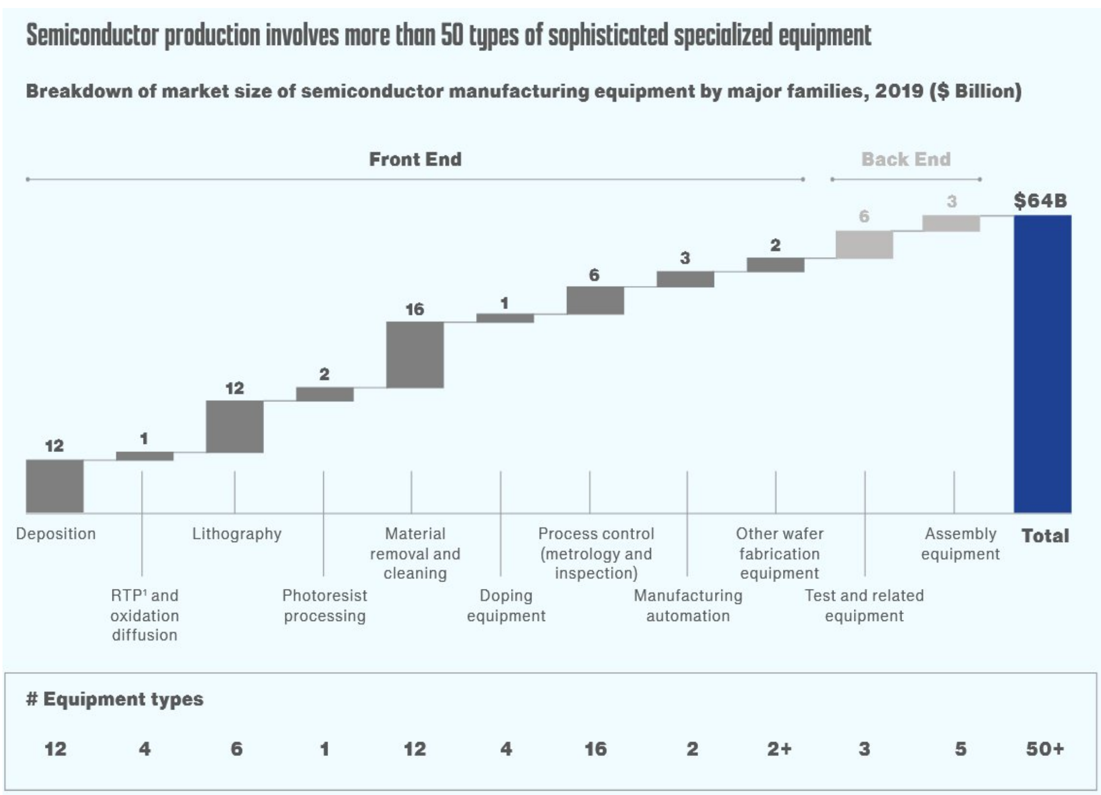

Figure 10 Breakdown of market size of semiconductor manufacturing equipment by major families (Source: BCG Analysis)

3.2.2 Factors deciding the location of Fabs

The location of semiconductor fabrication facilities is determined by a combination of infrastructure readiness, resource reliability, ecosystem depth, and state support, all of which directly reflect the capital-intensive and process-sensitive nature of fabrication.

3.2.2.1 Availability and Reliability of Critical Infrastructure

Given the extreme sensitivity of fabrication processes and their huge resource dependence, fabs require uninterrupted access to high-quality infrastructure such as continuous and stable power supply, large volumes of ultra-pure water, ecosystem to provide cleanroom-supporting utilities such as HVAC systems, vacuum systems, and waste treatment facilities and highly-connected transport and logistics networks. Fabrication facilities require large, contiguous land parcels with pre-developed infrastructure. Land parcels with industrial-grade zoning and clear land titles, and having proximity to transport and logistics networks (ports, highways, airports) are preferred.

3.2.2.2 Skilled Workforce and Technical Ecosystem

The fabrication process is highly complex and technologically demanding, thus requiring a technically skilled and innovative workforce, such as those trained in process engineering, materials science, etc. Locations with strong STEM education ecosystems and those provide mid- and high-skill technical labour are preferred by firms. In contrast to the design segment, fabrication relies not just on high-end research talent but also on a large base of operational and technical workforce.

3.2.2.3 Proximity to Supporting Industrial Ecosystem

Fabs also prefer proximity to key ecosystem players, such as equipment maintenance and servicing providers, materials and specialty chemicals suppliers,etc., since it improves efficiency and reduces overall time and costs of operation. Firms also prefer regions with existing semiconductor or electronics manufacturing base, since these regions offer lower operational costs, faster turnaround times and easier knowledge and technology spillovers. This explains the clustering of fabs in regions such as East Asia.

3.2.2.4 Government Policy and Financial Support

Given the high capital intensity and long gestation periods, state support plays a decisive role in fab location decisions. Locations with government support such as capital subsidies and tax incentives, regulatory facilitation and single-window clearances, easier and affordable access to infrastructure and utilities such as power, water, land, digital infrastructure, etc. and a long term policy stability are preferred. In many cases, public support significantly reduces financial risk and improves project viability, making it a key factor in attracting fab investments.

3.2.2.5 Market Access and Geopolitical Considerations

While fabs are globally integrated by their upstream and downstream supply chains, firms also consider access to major end markets such as electronics, automotive, defence, etc. to absorb the fabs' output chips, geopolitical alignment and supply chain security, and trade policies and export controls while setting up their fabs. Increasingly, countries are promoting domestic fabrication capabilities to reduce external dependencies, making strategic and geopolitical considerations central to location decisions.

3.2.3 Geographic distribution of Fabrication Segment

3.2.3.1 Wafer Fabrication Facilities

Due to advances in Moore's Law, it becomes efficient and cost-competitive to have more number of smaller transistors on chips, and thus efficient to imprint more number of chips per wafer, thus making the usage of 300mm wafers more cost convenient than the 200mm wafer. While this holds true for advanced chips, legacy chips (generally those having transistors of size 28nm, 40nm, 90nm, etc.) still find their applications in automotives, consumer electronics, and other major sectors, thus making wafer fabs with capabilities of using 200mm and 300mm wafers equally sought after (Thadani & Allen, 2024).

As of 2021-2022 data, out of the 1470 wafer fab facilities in the world, around 75% are in the Indo-Pacific countries, while the remaining 25% are in the USA, Europe and rest of the world. China holds the highest share with 24%, with Taiwan having 18% and Japan and South Korea at 17% each. This number is predicted to change in the coming years, with China's share is expected to reduce less than 24%, while the shares of South Korea and USA are expected to increase.

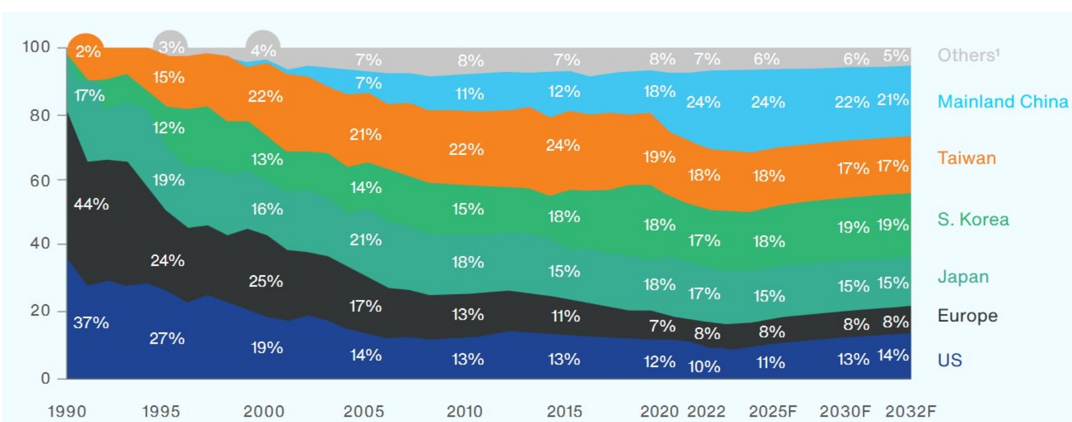

Figure 11 Global 200mm+ semiconductor fab capacity share by region, 1990-2032 (forecasted)

(Source: BCG Analysis)

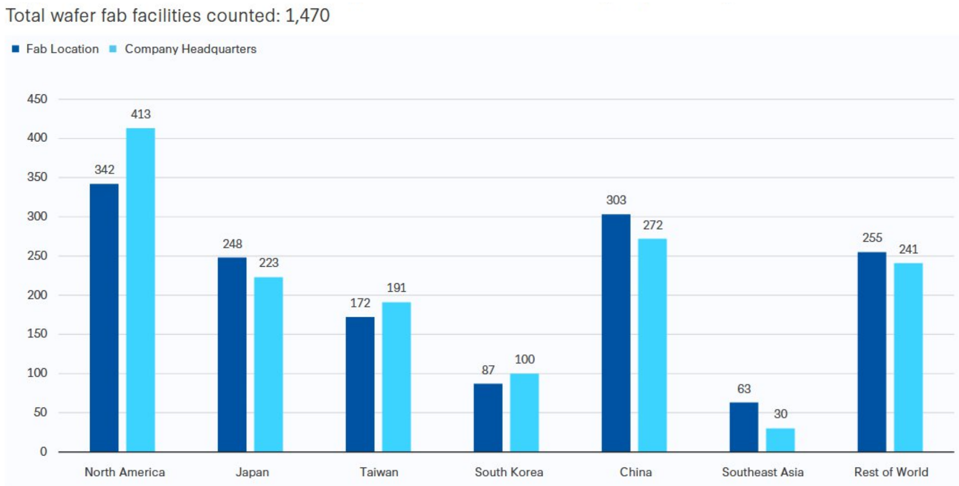

Figure 12 Number of wafer fabs by fab location and company headquarters

(Source: CSIS)

Out of China's total fabs, firms headquartered in the USA, South Korea, Japan and Taiwan operate a few. US firms operate 11 fabs in China, South Korean firms operate 11 fabs in China and Taiwanese firms operate 13 facilities in China. Apart from this, Chinese firms have also started investing in and building their own fabs in China.

3.2.3.2 Chemicals and Materials

Figure 13 Market size and number of major vendors by semiconductor materials segment

(Source: BCG Analysis)

Silicon wafers constitute the largest portion of the materials market, and around one-third of the total semiconductor materials sales in 2021. In 2020, the number of companies that can produce this critical component were only 5 and they controlled roughly 95 percent of the market. Silicon wafers with a diameter of 300 millimeters (these are the industry standard inputs) are supplied by firms headquartered in Japan, Taiwan, Germany, and South Korea.

Shin-Etsu, a Japanese company, is the largest silicon wafer manufacturer in the world, with a global market share of 29.4% in 2020. Likewise, Sumco (headquartered in Japan), GlobalWafers (headquartered in the United States), Siltronic (headquartered in Germany), SK Siltron (headquartered in South Korea), and Soitec (headquartered in France) together make up 65 percent of the global silicon wafer market. SK Siltron is leading the research and production in compound substrates such as Silicon Carbide (SiC) for its applications in emerging technologies such as EVs and Renewable Energy Systems. It is worth noting that Chinese firms have very little market share in this segment, and many Chinese companies are investing heavily in 300mm wafer production.

Other major companies in the overall chemicals and materials subsegment are Fujifilm (headquartered in Japan), DuPont (headquartered in the USA), Merck (headquartered in Germany), Linde (German company headquartered in UK) and BASF (headquartered in Germany). Japanese, Taiwanese, and South Korean firms dominate the supply of photomasks and photoresists. Here also, China's ability to produce advanced photomasks and photoresists is limited. China is investing significantly in this area also. In other precursor materials also, nations that lead are Japan, South Korea, the USA or their allies (Castané et al., 2025; Thadani & Allen, 2024)

3.2.3.3 Semiconductor Manufacturing Equipment (SME)

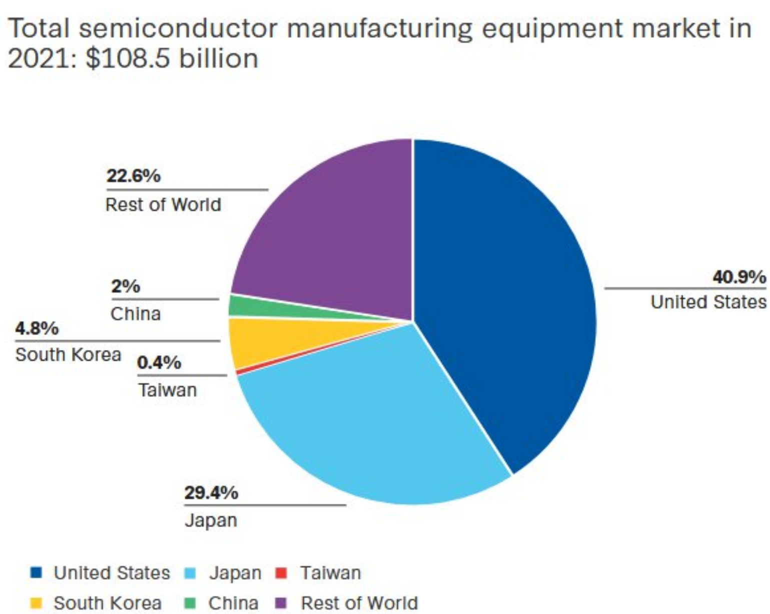

Figure 14 Semiconductor manufacturing equipment market share by company headquarters (2021)

(Source: CSIS)

US firms alone capture around 40% of the global SME market share followed by Japanese firms, which capture around 29%. The Netherlands has a huge share as well, so does

South Korea. South Korean SME is small but technologically sophisticated, making it an unmissable player in this sub-segment. Co-operation and Development, 2025; Precedence Research, n.d.; Thadani & Allen, 2024).

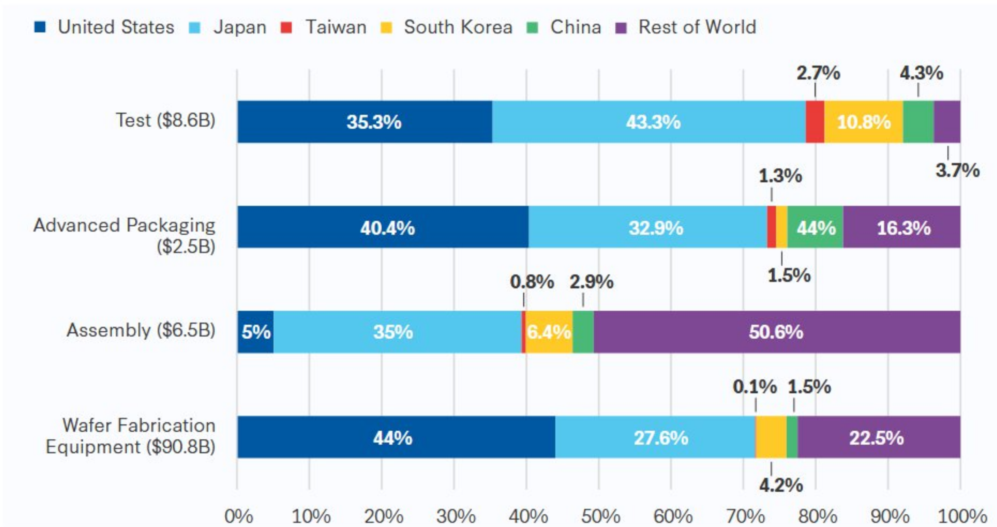

Figure 15 Semiconductor manufacturing equipment market share by company headquarters (2021), by SME category (Source: CSIS)

The wafer fabrication equipment sub-segment is led by the USA, followed by Japan and Netherlands. Major companies here are ASML (Netherlands based), Canon (Japan based), Nikon (Japan based), KLA Tencor (US based), Applied Materials (US based), Lam Research (US based) (Organisation for Economic Co-operation and Development, 2025; Precedence Research, n.d.; Thadani & Allen, 2024).

In the assembly equipment market, countries like Japan, Hong Kong, Singapore and Netherlands have a bigger share of the global market, with firms such as ASM Pacific Technology (Hong Kong based), Kulicke & Soffa (Singapore based) and BE Semiconductor Industries (Netherlands based) being the market leaders.

Japan holds around 43.3% of the global market share in test equipment, followed by the USA with 35.3% and South Korea with 10.8%%. Advantest (Japan based) and Teradyne (US based) are the major players in this test equipment market.

In the packaging equipment market, USA, Japan and Hong Kong are the market leaders, with firms such as Applied Materials (US based), Tokyo Electron (Japan based) and ASM Pacific Technology (Hong Kong based) being the market leaders (Organisation for Economic Co-operation and Development, 2025; Precedence Research, n.d.; Thadani & Allen, 2024)

3.3 Assembly, Testing, Marking and Packaging (ATMP)

After fabrication, the wafers are cut into individual chips. At this point, the individual chip which is essentially the functional block of semiconducting material is called a die. The dies are sliced from the wafers along the scribe lines. Prior to slicing, processes such as laser marking the dies, wafer probing to identify the good dies from bad dies, wafer thinning to reduce the thickness of the wafer to enable stacking of dies in packaging process, etc. are done. Placing these individual dies onto protective packaging and further processes to enable connecting these chips with other physical components of an electronic device, providing additional wirings, etc. are done in this ATMP stage (Accenture, 2024; Umbrex, n.d.)

Once the packaged and marked chips are ready, they are put into testing for real-world simulations. Intense testing for their efficiency, power leakages, performance, etc. are done. This is followed by a round of quality checking which includes processes like X-ray microscopy and acoustic microscopy to identify if any defects are present in the chips. These finalised chip products are sent to consumers such as Original Equipment Manufacturers (OEMs) who then integrate these chips into their products such as smartphones, automobiles, etc (Accenture, 2024; Umbrex, n.d.).

3.3.1 Key Characteristics of ATMP Segment

3.3.1.1 Lower Capital Intensity Relative to Fabrication

Compared to fabrication, ATMP operations require significantly lower capital investment. Although firms still invest in specialized equipment and facilities, the scale of investment is far lower than the USD 5–20 billion required for fabs.

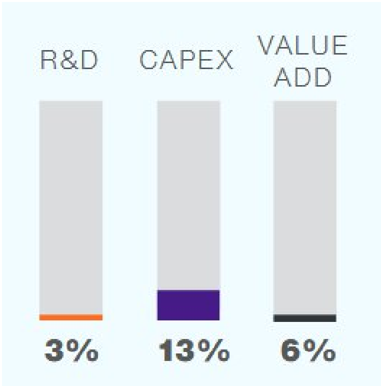

Figure 16 Key characteristics of ATMP segment

(Source: BCG Analysis)

At the industry level, ATMP accounts for around 6% of total value-add and around 13% of total CapEx**.** This relatively lower capital requirement makes the segment more accessible to a wider range of firms and countries.

3.3.1.2 Labour-Intensive Operations

ATMP processes involve a higher degree of manual and semi-automated work compared to fabrication. Activities such as packaging, inspection, and testing rely on a large operational workforce, making labour availability and cost key determinants.

3.3.1.3. Increasing Technological Complexity

Despite traditionally being considered a lower-technology segment, ATMP is becoming more sophisticated due to advances in chip architecture. Technologies such as 2.5D and 3D packaging, advanced system-in-package (SiP) designs and chiplets are increasing the technical requirements of this segment. This is leading to greater automation, higher precision requirements and increasing overlap with fabrication capabilities. As a result, fabrication facilities are increasingly providing ATMP services along with fabrication services also. For example, TSMC's Chip-on-Wafer-on-Substrate (CoWoS) method of 2.5D/3D packaging technology is increasingly being offered by TSMC fabs.

3.3.2 Factors deciding the location of OSAT facilities

Since OSAT facilities are more labour-intensive and less capital intensive, which often result in relatively low-skilled jobs (compared to fabs and design segment), regions with competitive labour costs and large pools of semi-skilled technical workers are preferred.

Additionally, these facilities are also becoming technologically more advanced, regions with mid- and high-skilled labour are preferred. Since ATMP is the final process in semiconductor production, regions with proximity to an existing base of end consumers of chips, such as electronics, automotive and defence industries are preferred.

3.3.3 Geographic distribution of Fabrication Segment

The ATP facilities are highly concentrated in the Indo-Pacific region. Most of them are in Taiwan, China and Southeast Asian countries, such as Vietnam, Philippines, Malaysia, Thailand and Singapore. Notably, China is increasing its investments in ATMP facilities more than any other country, followed by the USA (Thadani & Allen, 2024; Varas et al., 2021).

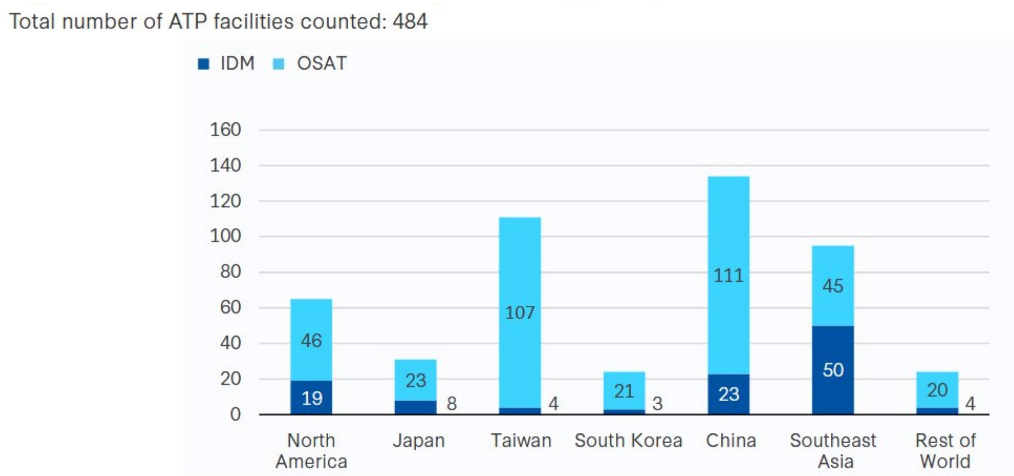

Figure 17 Number of ATP facilities per country (2021)

(Source: CSIS)

3.4 The Semiconductor Global Value Chain

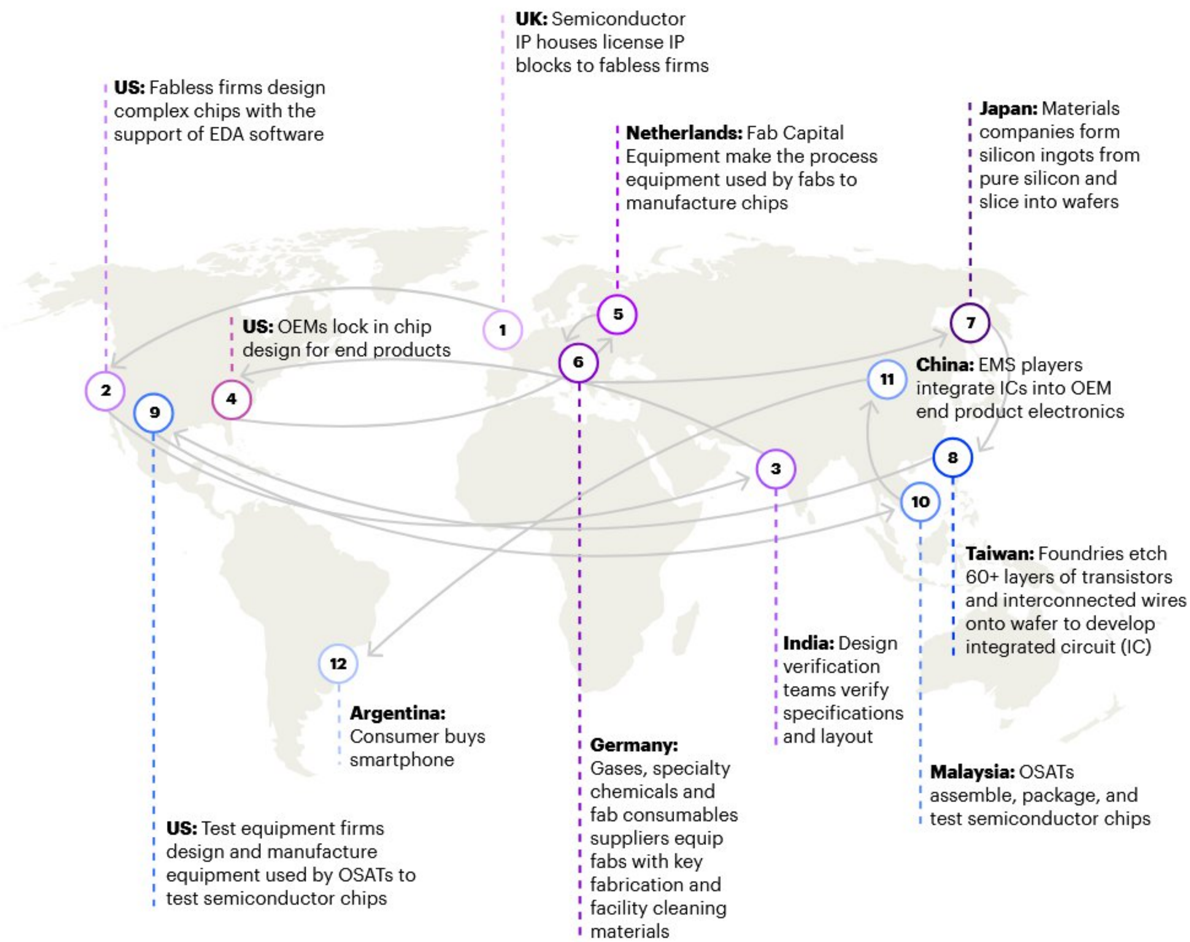

Figure 20 Semiconductor global value chain

(Source: Accenture)

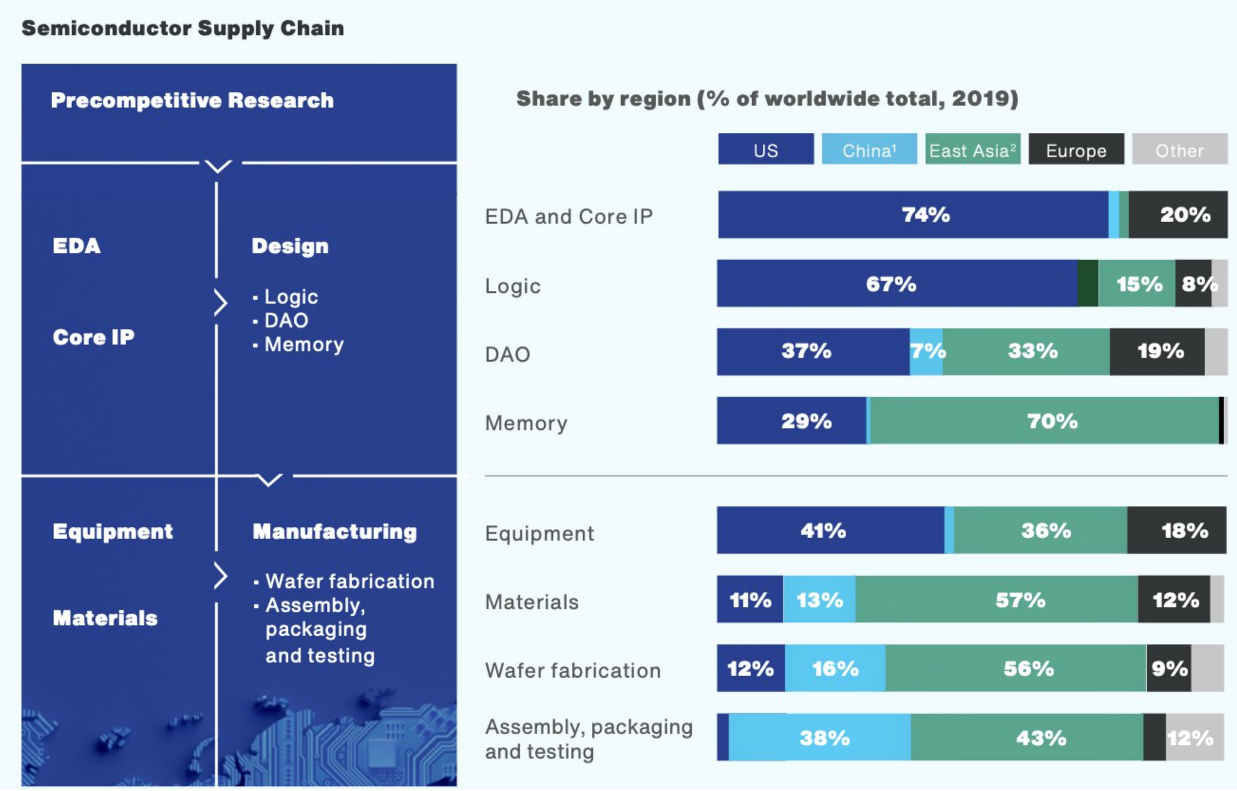

Figure 21 Global Semiconductor Supply chain

(Source: BCG Analysis)

The above images summarize the global distribution of the semiconductor industry value chain, making its production one of the most complex coagulations of goods and services.

4. The Semiconductor Value Chain as a Structural Hierarchy

Segment	**CapEx**	**R&D Intensity**	**Value Added**	**Entry Barrier**	**Leading Countries**
Design (EDA, IP, Fabless)	Low (relative)	Very High	~50%	High (human capital, ecosystem depth)	USA, UK

Fabrication (Fabs)	Very High (USD 5 - 20 billion per fab)	High	~24%	Extremely High (capital + tech barriers + infrastructure)	Taiwan, South Korea, USA
ATMP (Assembly, Test, Packaging)	Moderate	Low - Moderate (increasing)	~6%	Moderate (lower capital, labour-intensive)	China, Taiwan, Southeast Asia
Equipment & Materials (SME, Chemicals, Wafers)	High (specialized)	Very High	Less (strategic control > value share)	Extremely High (oligopolistic, tech barriers)	USA, Japan, Netherlands

Table 1 Semiconductor value Chain as a Structural Hierarchy

(Source: Author)

The semiconductor value chain is not uniform but is structured as a hierarchy of interdependent segments, each governed by distinct economic and technological factors.

At one end of the spectrum, the design segment is characterized by high R&D intensity, low physical capital requirements, and disproportionate value capture. This segment's dominance by a few countries reflects their deep investments in human capital, intellectual property, and innovation ecosystems, thus making it difficult for new entrants to capture a share of the market.

At the other end, the fabrication segment represents the most capital-intensive and infrastructure-dependent segment (including materials, chemicals and SME). Despite capturing a relatively smaller share of value, this segment requires massive upfront investment, long gestation periods and lead times, and increasingly advanced technological capabilities. These characteristics make this segment a triangulated paradox – a critical enabler of the value chain yet geographically concentrated with high entry barriers, making it difficult for its geo-diversification.

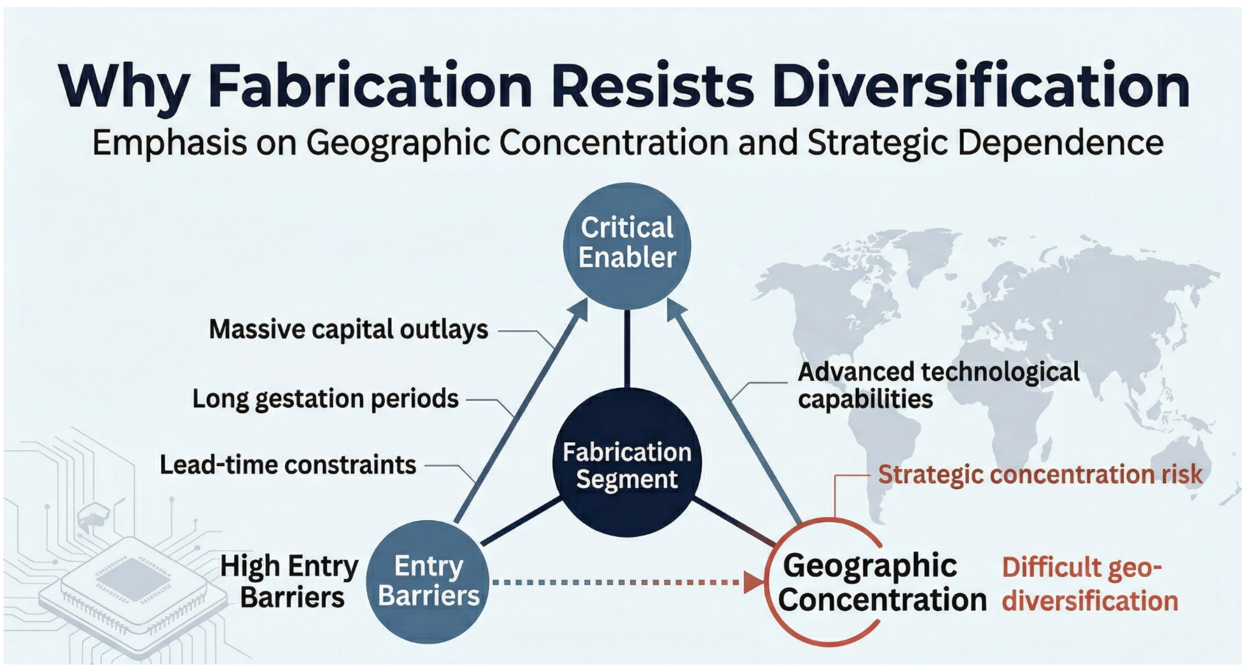

Figure 22 Why fabrication resists diversification

(Source: Author)

The ATMP segment, in contrast, occupies an intermediate position. With relatively lower capital requirements and higher labour intensity, it has historically served as an entry point for latecomer economies. However, increasing technological complexity in advanced packaging is gradually raising the barriers to entry in this segment as well.

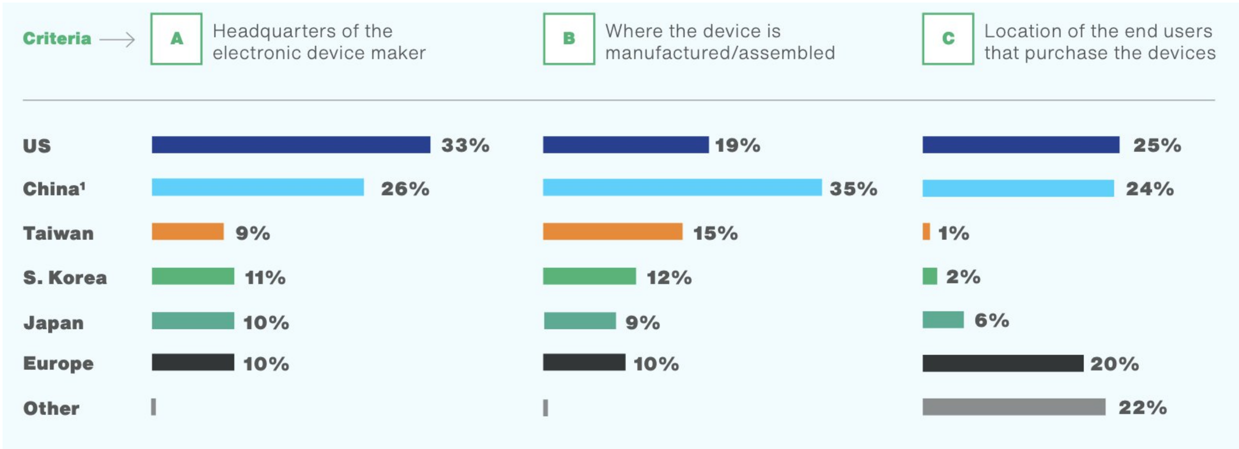

Figure 23 Global semiconductor sales by geographic area, 2019

(Source: BCG Analysis)

As seen from the above image, the demand and supply for semiconductors is fragmented, implying that no country participates uniformly across the semiconductor industry. This implies that national strategies are shaped by selective entry into specific segments of the value chain, depending on their existing resource capabilities and constraints, and strategic priorities.

5. Research Gap

As illustrated in global value chain mappings, India is already present in this ecosystem – primarily in design services – but captures only a marginal share of overall value. And the domestic and geopolitical scenarios have directed the policy attention towards bringing more fabs and OSAT facilities, and increasing the Design segment's share of the country – through fiscal incentives, infrastructure development, skill development, etc. However, this framing overlooks a more fundamental question:

> How can India strategically position itself within an already mature, highly fragmented, and geographically concentrated global semiconductor value chain?

Addressing this gap requires moving from the debate on needing domestic fabrication towards a segment-specific strategic framework, which evaluates India's potential entry points across the semiconductor value chain based on structural characteristics, entry barriers, and global competitive dynamics.

6. Research Questions

1. What are the key challenges in India's STI and industrial ecosystems that act as barriers to achieving semiconductor self-sufficiency?
2. What key lessons can India learn from global best practices for overcoming these challenges?

7. Methodology

This study employs a qualitative research design to explore the challenges and reforms needed in the STI (Science, Technology, and Innovation) and industrial ecosystems for semiconductors. It draws on expert insights and policy analysis to develop practical, actionable policy recommendations. To organize the analysis, this study uses a three-pillar analytical framework, namely – Technology, Industry, and Geopolitics to examine how these 3 forces interact and shape national and international semiconductor strategies.

7.1 Approach and techniques

The primary qualitative techniques used are:

- Document analysis: Systematic review of policy documents, reports, and strategic initiatives from India (e.g., India Semiconductor Mission) and leading countries (e.g., Made in China 2025, U.S. CHIPS Act).

- Case studies: In-depth examination of successful reforms in STI and industrial ecosystems, focusing on countries that have built strongholds in critical semiconductor technologies.

7.2 Methods of data collection

Data collection relies exclusively on secondary research, leveraging publicly available sources for efficiency and accessibility. Key sources include:

- Official policy documents and government reports from India and comparator countries.
- Academic literature, industry analyses, and think-tank publications on global best practices in semiconductor ecosystems.
- Expert interviews or commentaries (where available in secondary form) to incorporate stakeholder perspectives.

8. Analytical Framework: Structural Drivers of Semiconductor Industry

The semiconductor industry is shaped by three mutually interacting pillars – technology, industry, and geopolitics – and understanding their interaction is essential for evaluating any country's semiconductor strategy.

8.1 Pillar 1: Technology

8.1.1 Technological Dynamics

The semiconductor industry follows the “winner-takes-all” and “first-movers advantage” principles. Like any other industry, this industry also has cut-throat competition, but due to the extremely limited knowledge and production capabilities present in the world today combined with the exponential growth in the demand for chips, and there seems to be even sharper cut-throat competition. Due to these reasons, even a slightest improvement in the technology or the service offered captures a huge share of the market revenue. This has pushed the firms to adopt continuous technological improvement to survive in the industry. This can be seen in how much percentage of the revenues do firms in this industry reinvest in their R&D. This dynamic also makes it difficult for competitors in the market to catch up with market leaders since the latter firms are years ahead in terms of technological improvement, and they reinforce their dominance through sustained R&D investment.

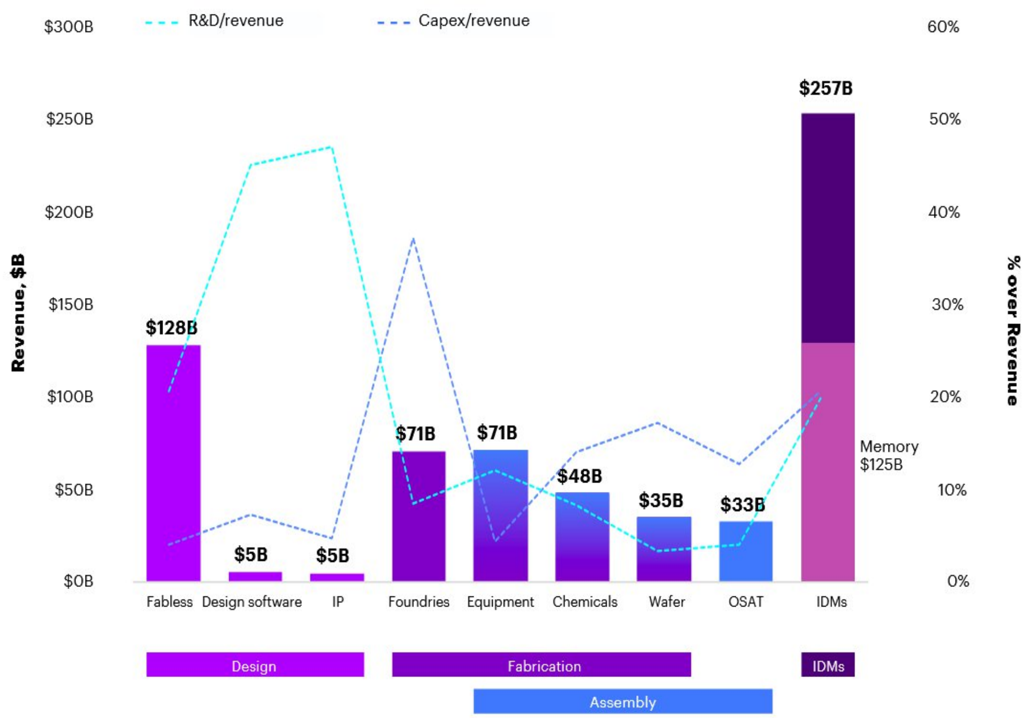

Figure 24 R&D and CapEx consumption as a share of semiconductor firms' revenues

(Source: Accenture)

8.1.2 State Support and Innovation Systems

In the semiconductor industry, precompetitive research constitutes around 15-20% of the industry's overall R&D. This involves basic but important research such as identifying the choice of chemicals for various processes, choice of fundamental materials for advancing the technology, etc. This basic research has a huge role in aiding the advancement of any technology. For example, the EUV technology – the only technology today capable of patterning and imprinting advanced nodes – took nearly four decades to be commercialized starting from a basic research idea.

For example, the analysis of total R&D investment across all the sectors in the USA provides some insights. In 2018, the US Federal government contributed to 42% of the funding for basic research while 30% was funded by state governments, universities and other non-profit research institutions. Only 28% of the funding came from companies. In contrast, companies funded 80% to applied research and development – the kind of advancements which typically follow after breakthroughs in basic research. Similar trends can be seen in major countries, such as China's and Japan's R&D ecosystem as well. These countries have higher contributions from the private sector in the R&D, while the government spends more on fundamental research.

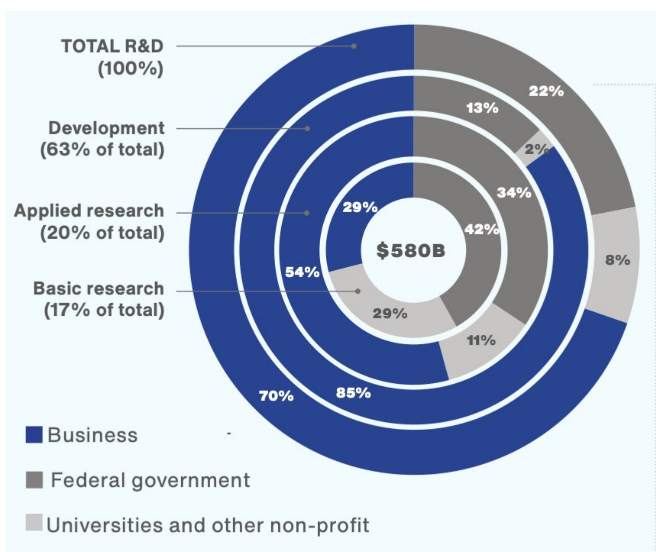

Figure 25 Total US R&D investment across all sectors, 2018

(Source: BCG Analysis)

Another example is how technological growth was promoted in China due to state support. Initiatives such as the National Hi-Tech R&D Program (863 Program) focused on identifying globally emerging technologies of strategic importance and supporting their coordinated development and industrial demonstration. Complementing this, the National Basic Research Program (973 Program) was aimed at strengthening the foundational scientific capabilities and fostering a culture of exploratory research in the society. The National Key Technologies Program was launched with the aim of developing "generic technologies" that benefit entire industries. It was instrumental in supporting massive national engineering projects like the Three Gorges Dam, the Qinghai-Tibet Railway, and the Beijing-Shanghai High-speed Railway (Consulate General of the People's Republic of China in Montreal, 2013).

8.1.3 Learning by Doing

Learning-by-doing is a foundational characteristic of the semiconductor industry, where mastering complex manufacturing processes (such as lithography and etching) requires practical, hands-on experience rather than just theoretical knowledge. This experiential learning allows for continuous process improvement, higher yield rates, and enhanced product quality.

This idea of Learning-by-doing is the primary economic justification for subsidies being used as the primary tool for attracting semiconductor investments. Preliminary estimates suggest that learning rates are smaller, approximately 3.4% to 8% only. Nevertheless, learning-by-doing has a significant role in improving the overall quality of the finished product and also helps in deepening the innovation process of people in this industry.

Significant learning occurs across borders rather than just within individual firms or countries. These spillovers are likely facilitated by fabless clients (like NVIDIA or Qualcomm) who intermediate knowledge globally by interacting with various foundries in different countries (Goldberg et al., 2026). This suggests that subsidies alone will not be sufficient for a country's semiconductor industry to thrive. Subsidies will work in countries that have an established industrial base for allied industries such as electronics, machinery, automobiles, etc. which will also act as consumers of the semiconductor chips that will be produced by the to-be setup fabs.

Technology alone, however, does not determine semiconductor competitiveness. The ability to generate and absorb technological advancement depends critically on the industrial ecosystems within which firms operate, and on the geopolitical scenarios that determine who gets access to frontier knowledge in the first place.

8.2 Pillar 2: Industry

8.2.1 Specialized Value Chain

Presently, no single country or company is capable of doing all the activities, from design to manufacturing to packaging. The market leader firms focused on one product or segment and specialized in terms of R&D and product development in that product segment. This is seen in the top players in each segment. Intel is the leader in the laptop and desktop CPUs, Qualcomm is the leader in the smartphone system-on-chip market, TSMC is the leader in the advanced chip manufacturing market, ASML is the leader in the lithography equipment market, Samsung leads the memory market and NVIDIA dominates the market for graphics cards. Japan leads in the specialty chemicals market while Japanese and South Korean companies lead in the wafers production market. The key trend here is: market leader firms focus on one product or segment and invest heavily in that segment. The semiconductor industry is a highly specialized value chain where competitive advantage is segment-specific rather than system-wide.

8.2.2 Role of Manufacturing Base in Driving Semiconductor Competitiveness

A strong domestic industrial base plays a crucial role in sustaining semiconductor capabilities. Given the fact that fabs have to operate at near capacity utilization and operate at economies of scale, presence of downstream industries such as electronics, automobiles, and telecommunications can generate stable demand for chips, enabling economies of scale and continuous production. This is visible in the case of China and Japan, whose domestic demand for chips grew because of their growing electronics, automobiles and telecommunications industries, thus driving investments into their semiconductor industry and improving their economies of scale.

Beyond demand generation, a robust industrial base also plays a crucial role in strengthening innovation outcomes. A robust electronics manufacturing sector will help validate new semiconductor technologies with less turnaround times, helping the overall innovation ecosystem. Also, today’s market leader nations started as electronics manufacturers and were able to move into the semiconductor industry owing to the experience and tacit knowledge they could gain in the electronics industry which could not otherwise be learnt through manuals or theoretical understanding.

Empirical studies also show the role of industrial depth in driving innovation. A report by the Information Technology and Innovation Foundation (ITIF) finds a very high correlation (correlation score of 0.62) between a nation's manufacturing strength (i.e., industrial base) and its overall innovation performance. The report says that manufacturing strength cannot be isolated from promoting innovation. Countries with strong hardware ecosystems – like Korea and China

– can move faster from downstream production to upstream idea generation than an idea leader with a weak manufacturing base can move from upstream to downstream (Atkinson et al., 2025).

WIPO's latest round of Global Innovation Index (which ranks 139 economies) ranks USA at 3rd, South Korea at 4th, China at 10th, Japan at 12th, India at 38th ranks, while Taiwan ranks higher in the world's major innovation clusters. These countries perform strongly on global innovation rankings because they have deep industrial bases that have the capability to turn research into products faster. In these systems, universities do not operate in isolation – they are connected to firms, suppliers, clusters, and commercialization channels that help ideas move from laboratory to market, which is seen in their manufacturing value added to their respective GDPs. South Korea, Japan, China and Taiwan have a higher share of manufacturing value added to their GDPs, according to the Composite Industrial Performance Index, released by the UN International Development Organization, which ranks countries based on their ability to produce and export manufactured goods competitively. USA scores 0.62, South Korea scores 0.72, China scores 0.61, Japan scores 0.79 and Taiwan scores 0.83, whereas India scores 0.37 (on a scale of 0 to 1, 1 being the highest) in the segment called "share of medium and high-tech manufactured exports share in their total manufactured exports". (United Nations Industrial Development Organization, n.d.). These correspond to the need of a strong electronics manufacturing base for the semiconductor industry to thrive in a country.

8.2.3 Cluster-Based Production Ecosystems and Agglomeration Advantages

Clusters have proven to work better for the overall semiconductor industry. Clusters are geographically concentrated ecosystems of manufacturers, suppliers, and skilled labor that create a mutually reinforcing environment. These clusters provide competitive advantages as they provide:

1. Specialized Labor Pools: They develop workers with niche industry-specific technical skills, often supported by local industry-oriented universities.
2. Supplier Linkages: Near proximity to suppliers creates economies of scale in production in the entire supplier ecosystem, while reducing cost of and redundancy of infrastructure.
3. Knowledge Spillovers: These clusters facilitate the exchange of ideas and tacit knowledge – the "know-how" gained through hands-on experience and observation rather than formal manuals.
4. Clusters provide hands-on experience of all segments in the ecosystem to all actors in the ecosystem, reducing the silos problem often seen in globalized and segmented operations.

The Hsinchu Science Park in Taiwan is cited as the preeminent example of a successful cluster, where a complete microelectronics ecosystem – wafer design and fabrication, EDA tools, fabless design firms, SME, Materials suppliers, ATP facilities – exists within walking distance, drastically reducing cycle times. Nearby are two world-class research universities – National Chiao Tung University and National Tsing Hua University, which has produced a large number of graduates for the companies and research organizations operating in the Science Park. For example, around 65% of Hsinchu Science Park’s top executives were graduates of the National Chiao Tung University in 2012. This has in turn aided knowledge spillover in the cluster – out of the approximate 1,50,000 employees in the Park, a major share of them had work experience in some aspect of semiconductor manufacturing. In 2024, South Korea launched the “World’s Largest and Best Semiconductor Supercluster Construction Plan,” proposing the construction of 16 new plants, including R&D facilities, and also constructing “Semiconductor Superclusters” in semiconductor-intensive cities such as Pyeongtaek and Hwaseong at an investment of around USD 454 billion by 2047.

Paradoxically, creating new greenfield clusters for semiconductors without historical industrial or educational advantages is difficult and has often shown to fail, thus reinforcing the importance of an existing electronics industrial base for knowledge transfer and relevant experience. Thus, the government should invest its resources in regions with existing infrastructure instead of investing in regions that have thin innovation ecosystems. (Shivakumar, 2023).

Yet industrial strength does not emerge in a vacuum. The depth of a nation's manufacturing base is shaped by deliberate state strategy and by the geopolitical relationships that determine market access, foreign investment flows, and technology transfer opportunities – the focus of the third pillar.

8.3 Pillar 3: Geopolitics

8.3.1 State Strategy & Techno-Industrial Policy

The presence of a large number of fabs, materials and chemicals suppliers and SME manufacturers in the Indo-Pacific region can be attributed to the industrial policy and innovation policies these countries adopted years ago. No single country has achieved a miracle in this semiconductor industry. Years of innovation and industrial process improvement has aided them in achieving the current scale of production, and integrating them well into the global value chain. Semiconductor competitiveness is the outcome of long-term techno-industrial policy and cumulative ecosystem development, not short-term capital infusion.

This is seen in Japan's emphasis on modernizing its industries, and China's Megaprojects, Strategic and Emerging Industries and Made in China 2025 policies, where industries were actively encouraged to invest in advancing their capabilities, by integrating technological improvements into them. Japan's techno-industrial strategy uses international collaboration along with its Private sector-University-State model, where the State will direct the strategic areas that need attention along with funding, while private firms pool in their resources thus reducing redundant efforts, and the nation's research institutes, labs and universities will provide technical support. One example is that of the Super LSI Technology Research Association, which was formed by Japan's 6 major computer firms with USD 300 billion funding support from MITI. The goal of this Association was to develop advanced fabrication processes, photolithography processes and more advanced DRAM technology. As a result, a new technology called Electron Beam Lithography (EBL) was invented by the Association. This EBL revolutionized the chip making process, paving the way for advanced nodes to be fabricated and later, this EBL was commercialized by ASML, Canon, Nikon (Tomoshige, n.d.).

In the case of China, the Megaprojects initiative, the Strategic and Emerging Industries initiative and Made in China 2025 initiative all focused on building the nation's industrial capabilities and turning the industries into engines of innovation. For example, the Made in China initiative specifically mentions "enhancing innovation capability of the manufacturing sector" and "integrating technology and industry" as some of the priorities which are important to developing China's manufacturing sector and improving the innovation capability (International Energy Agency, n.d.; Nair, 2022).

Technologically advanced countries do not see technological improvement as a separate vertical – technological growth is seen as a national priority, and all major policies are directed towards integrating technology with various sectors of the economy. The trend the Asian economies followed for their technological advantage is broadly defined as:

Export oriented manufacturing and Large industrial base → exposure to competition → survival-driven innovation push → deliberate search for knowledge inside and outside the firms → institutionalized market-technology linkages

8.3.2 Subsidies – the major policy tool

Government support throughout every stage in this industry has played a significant role in positioning today's leading countries' industrial and technological development. While governments previously allowed the private sector to lead in mature markets, there has been a significant increase in government intervention since 2020. Major producers, including the US, China, Japan, and South Korea, have notably ramped up financial support since the COVID-19 pandemic. Private investments are also steady and increasing, but the high upfront costs of establishing the industry ecosystem is supported by government support. Subsidies are often in the form of financial grants, tax incentives, loans, loan guarantees, and equity injections.

The US CHIPS Act has a financial outlay of USD 52 billion, out of which USD 39 billion for building or expanding semiconductor fabs and USD 13 billion dedicated to semiconductor research, development, and workforce training. A 25% investment tax credit is given to companies building their semiconductor manufacturing facilities in the USA (Sacks, 2024).

The Big Fund of China (as part of its National IC Guidelines) has disbursed equity funds totalling worth USD 142 billion in the 3 iterations it has been implemented so far. Apart from this, local and provincial governments have also been encouraged to raise their sources of funds to fund new semiconductor facilities.

The European Chips Act (part of EU's Digital Compass 2030 Strategy) has an outlay of USD 47 billion in the form of grants, loans, aid, tax credits and state aid. South Korea's K-Belt

Semiconductor Strategy offers USD 55 billion in tax incentives, under the K-Chips Act (Varas et al., 2021).

Japan launched its Semiconductor and Digital Industry Strategy in 2021 with a financial outlay of USD 17.5 billion in grants, mainly to fund its advanced R&D institute, Leading-Edge Semiconductor Technology Center and to fund the nation's new semiconductor venture, Rapidus. Taiwan's Angstrom Initiative and Moonshot Project have pledged funds worth USD 16 billion in the form of tax incentives, subsidies and tax credits (Varas et al., 2021).

8.3.3 Cross-Border Technology Transfer and Capability Catch-Up

Cross-border technology transfer is as crucial as state support for industrial development. Outside of the United States, there is no instance where a domestic semiconductor industry developed without substantial foreign technology acquired through FDI, research collaborations, or licensing. This explains why China has struggled to reach the technological frontier despite massive spending since US allies and other East Asian economies had far better access to foreign frontier technologies (Goldberg et al., 2026). Tech transfer has played a crucial role in today's market leaders, like Japan, South Korea and Taiwan.

8.3.4 Geopolitics and geoeconomics drive strategic decisions

Geopolitics and geoeconomics are at the core of today's market leaders' success, namely Taiwan, South Korea, Japan and China. Although the initial support these countries received was from the Western countries (mainly the USA), their sustained engagement with the USA was beyond being geopolitical – they proved to be strong economic partners to the USA, thus turning the dynamic to be geoeconomic as well. Japan, South Korea and China have been greatly benefited by their access to a vast market – these countries' industries developed owing to the export oriented model which gave their industries continued support and capital.

For Japan and South Korea, preferential access to the US market meant that their industries could keep producing while improving their quality of products since they were catering to the American consumers. For China, the world was the customer – Chinese firms expanded the diversity of their offerings to the world, thus becoming the factory of the world. This gave Chinese companies huge profits which the State used to reinvest in indigenous innovation. Semiconductor supply chains are embedded in geopolitical and geoeconomic alliances, not just market forces.

The US supported Japan post WW2 as a part of its "offshore island" strategy – to keep Japan as a critical industrial and geopolitical asset in East Asia. The US helped Japan technologically and industrially by transferring management and production know-how, by providing security and market conditions and access to the American market that made domestic investment possible, and by letting Japan import and absorb foreign technology at scale. This greatly helped Japan dedicate its resources towards reconstruction and development. The exports also earned crucial foreign exchange, which the government used to import advanced foreign technology to be used to modernize their domestic industries (Giorcelli et al., 2025; McGlade, n.d.; U.S. Department of State, n.d.).

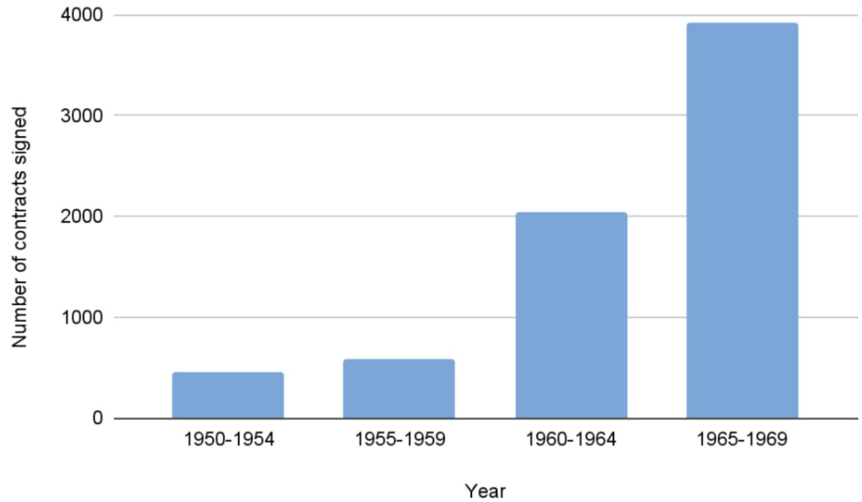

Figure 26 Number of contracts Japan signed to import new technology between 1950 and 1969

(Source: Berkley Economic Review)

To reduce its dependency on a single country and as a part of its "offshore island strategy", the USA cultivated firms in countries like South Korea. US firms like Micron and Texas Instruments licensed key designs to Samsung and SK Hynix to create a counterweight to Japan. For example, between 1982 and 1986, the United States provided 36 out of 53 (68%) of South Korea's total semiconductor technology transfer contracts. And by 1985, major South Korean firms like Samsung, LG, and Hyundai had established operations in Silicon Valley, investing a combined USD 1 billion to facilitate the acquisition of modern technology, staff training, and business coordination with American partners (Mushkudiani, 1999).

A contemporary example of geopolitics at play would be the case of Rapidus, Japan's centerpiece for reviving its semiconductor industry. Japan's major firms are partnering with IBM and the European research hub IMEC to develop advanced 2nm technology which are aimed to be produced in Japan's upcoming fabs, which are majorly being built by TSMC. The 2023 rules of METI's Semiconductor Strategy emphasises on collaboration with the USA, the EU, South

Korea, Taiwan, the Netherlands, the UK and Belgium, and these efforts are complementary to the efforts of the “Fab 4” initiative, a US led initiative to strengthen the semiconductor supply chain in the Asia-Pacific region, which includes South Korea, Taiwan and Japan (Shivakumar et al., 2024).

Taken individually, each of these three pillars offers only a partial explanation of semiconductor competitiveness. It is only when viewed together – as a mutually reinforcing system – that the full picture emerges. The following section examines how technology, industry and geopolitics interact and amplify each other, and what that means for any country seeking to build semiconductor capabilities from scratch.

8.4 The Three Pillars as a Mutually Reinforcing System

The three pillars of technology, industry, and geopolitics do not operate in silos. They form a mutually reinforcing system where each pillar shapes and is shaped by the other two. The historical trajectories of today's semiconductor leaders make this interdependence visible.

Geopolitics creates the conditions for industrial development and technological catch-up. The US decision to support Japan post-WW2 through its "offshore island strategy" gave Japan preferential access to the American market and foreign technology. This geopolitical arrangement allowed Japan's industrial base to scale up through export-oriented manufacturing, which then generated the adequate knowledge necessary for technological advancement.

The same dynamic explains South Korea's rise. US firms licensed key semiconductor designs to Samsung and SK Hynix not only because of commercial reasons, but as a geopolitical counterweight to Japan. This technology transfer gave South Korea a foundation to build on industrially, which it then reinforced through cluster development in cities like Pyeongtaek and Hwaseong, and sustained through long-term state strategy.

The interdependence also runs in the other direction – technology and industry shapes what geopolitics can achieve. Taiwan's Silicon Shield illustrates this clearly. TSMC's advanced chip manufacturing capacity has made Taiwan geopolitically indispensable – major powers, including the US, are compelled to provide support to Taiwan because the world's most critical semiconductor infrastructure sits on the island.

Finally, industry mediates the relationship between geopolitics and technology. Countries with deep industrial bases, like South Korea and Japan, can absorb and commercialize technology faster because their manufacturing ecosystems are connected to universities, suppliers and downstream industries. This is why industry acts as the transmission mechanism through which geopolitical access to technology becomes actual technological capability.

In sum, semiconductor competitiveness is not the product of a single pillar, but an outcome of geopolitical positioning enabling tech sharing and industrial development, industrial depth enabling technological learning, and technological and industrial capabilities reinforcing geopolitical leverage.

9. India's place in the semiconductor value chain

9.1 India's need for semiconductors

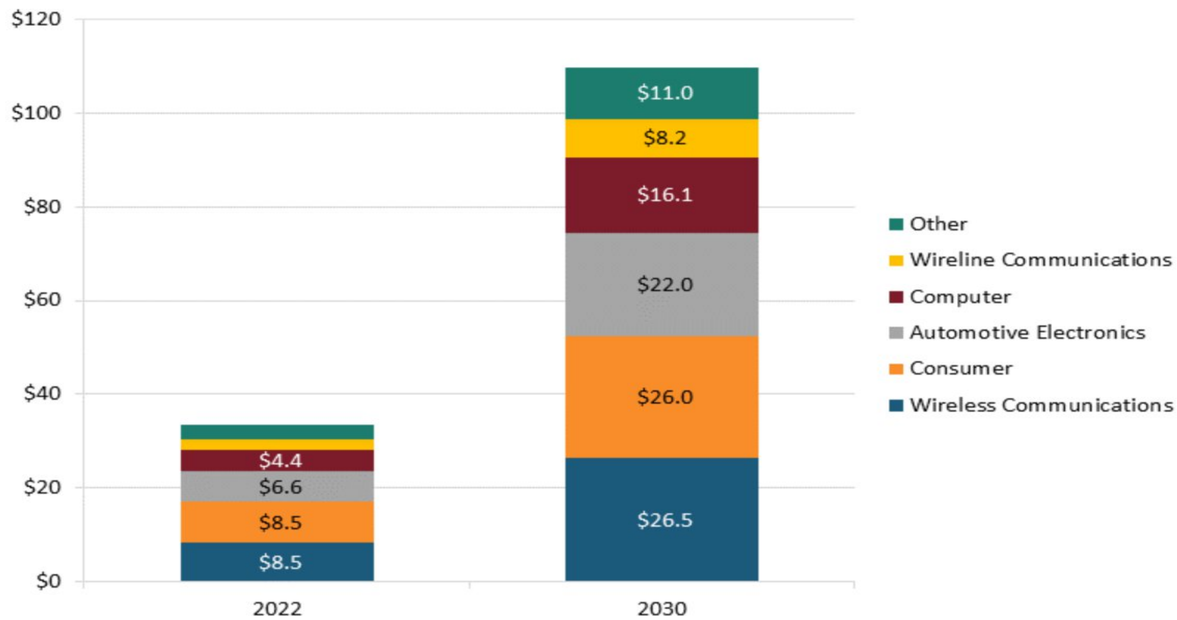

Figure 27 India's semiconductor market, 2022 (actual) and 2030 (forecast) (in USD billions)

(Source: ITIF)

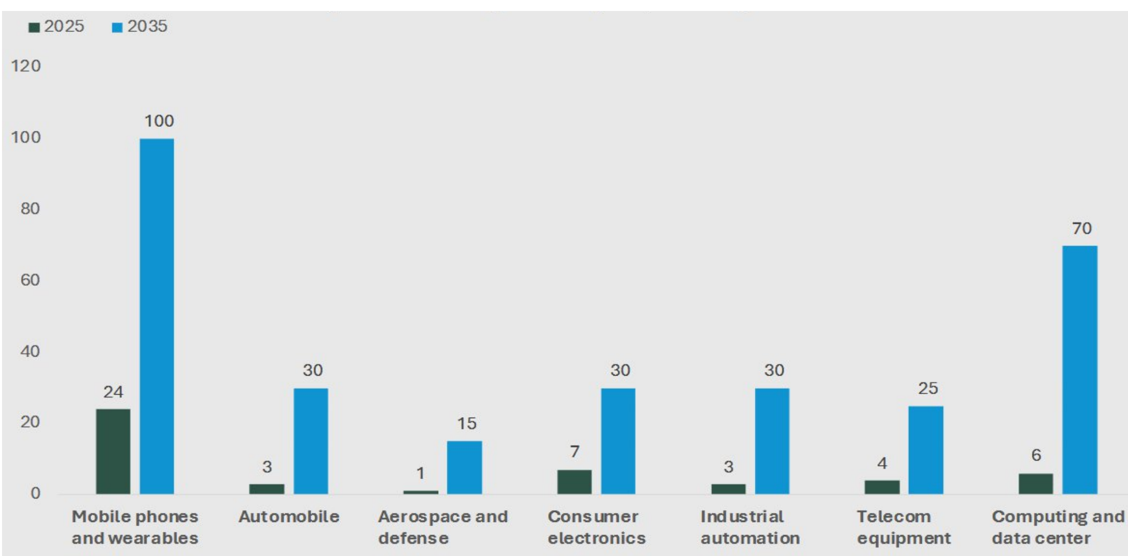

Figure 28 India's semiconductor market by end-use segments (in USD billions)

(Source: Deloitte)

India’s semiconductor market is expected to reach USD 120 billion by 2030 and USD 300 billion by 2035. Major factors driving this growth are the increased adoption of AI, automobiles and data centers.

The increased adoption of AI in everyday lives has placed a higher demand on the computational capabilities of data centers, servers and edge devices, with a combined worth of at least half a trillion USD. India saw a cumulative investment of USD 60 billion in its data centers segment, during the 2019-2024 period. During 2024 alone, India’s data center segment saw investments worth USD 19 billion. Between 2025 and 2027, this segment is expected to attract an additional USD 45 billion investments, driven by increasing cloud computing and cloud storage services, HPC requirements, etc. India’s data center capacity is expected to grow from around 1.5 GW in 2025 to 10 GW by 2030 (Deloitte India, 2026).

India’s electronics manufacturing segment is predicted to reach USD 500 billion by 2030, with USD 350 billion of finished goods and USD 150 billion in components manufacturing. India is also expected to remain in the top three electronics manufacturing hubs in the world by 2035. India’s mobile phone manufacturing segment (worth USD 64 billion in FY2025) is the second-largest in the world. Since semiconductors account for around 30% of smartphones’ total cost (in terms of Bill of Materials), smartphones are a key driver of semiconductor demand in India (Deloitte India, 2026).

With higher adoption of latest technologies such as ADAS, electric powertrain modules, smart connectivity features, etc. in the latest automobiles, the total cost of chips used in automobiles is expected to increase from USD 600 per vehicle in 2025 to USD 1200 in 2030. India’s EV penetration rates are also expected to increase, from the current 7.8% to 30% by

2030 and more than 60% by 2035, thus driving the domestic demand for semiconductors (Deloitte India, 2026).

Apart from these, other segments such as the consumer electronics, aerospace and defence industries, industrial automation and telecom equipment are expected to play crucial roles in driving India's demand for semiconductors. But, India currently imports around 90% of its semiconductors mainly from China and Japan, thus placing the nation's rising manufacturing sectors at a chokepoint (Deloitte India, 2026).

9.2 India's policies for semiconductors and electronics industry

9.2.1 Semicon India Programme / India Semiconductor Mission

With an initial outlay of Rs. 76,000 crores, India launched the Semicon India Program in 2021 to coordinate the development of semiconductor fabs, display fabs, compound semiconductors, ATMP/OSAT facilities, and chip design facilities. India's semiconductor policy architecture has 4 main pillars:

1. **Semiconductor Fabs Scheme**: This scheme provides up to 50% fiscal support for setting up semiconductor fabs in India. It targets mature nodes as well as advanced nodes (such as 28nm or below).
2. **Display Fabs Scheme**: This scheme provides fiscal assistance of up to 50% of the project cost to set up display fabrication units in India.
3. **Scheme for Compound Semiconductors and OSAT Facilities**: This scheme supports the setting up of units for compound semiconductors, silicon photonics, MEMS/sensors, and discrete semiconductors. It also offers financial support upto 50% for setting up ATMP/OSAT facilities.

4. **Design Linked Incentive (DLI) Scheme**: With a dedicated outlay of Rs. 1000 crores, this scheme promotes semiconductor design startups and MSMEs by offering financial support across product development stages. The scheme includes reimbursement of R&D costs, access to state-of-the-art design tools (such as those offered by C-DAC) and incentives up to Rs. 15 crore per company to encourage innovation in chip design.

As of December 2025, 10 projects worth Rs. 1.60 lakh crores had been approved under ISM – 2 fabrication units and 8 ATMP facilities across Gujarat, Odisha, Uttar Pradesh, Punjab, Andhra Pradesh. These include CMOS silicon fabs, silicon carbide fabs, advanced and memory packaging units. Among these projects, Micron Technology is setting up an ATP facility in Gujarat and Tata Electronics is setting up a major semiconductor fab in Gujarat in collaboration with Powerchip Semiconductor Manufacturing Corporation (PSMC) of Taiwan (Prasada, 2026; Press Information Bureau, 2025).

Apart from these, a new curriculum on VLSI Design and Technology and IC manufacturing has been introduced by the AICTE and the Skilled Manpower Advanced Research and Training (SMART) Lab has been established at the National Institute of Electronics and Information Technology (NIELIT), Calicut to train 1 lakh engineers nationwide in addition to the 44,000 plus engineers already trained. Partnerships with Lam Research, IBM and Purdue University have been signed for upskilling India's engineers and advancing R&D in AI and advanced semiconductor technologies (Prasada, 2026; Press Information Bureau, 2025).

9.2.1.1 India Semiconductor Mission 2.0

In India's Union Budget 2026-27, the Indian Semiconductor Mission 2.0 was announced with an outlay of Rs. 1000 crores. ISM 2.0 focuses on producing materials and semiconductor equipment in India, and developing a full-stack Indian semiconductor intellectual property.

Along with this, the Budget also saw the launch of the Modified Programme for Development of Semiconductor and Display Manufacturing Ecosystem in India with a financial outlay of ₹8,000 crore (Press Information Bureau, 2026).

9.2.2 Electronics Components Manufacturing Scheme (ECMS)

Launched in 2025 with an outlay of Rs. 22,919 crore (equivalent to USD 2.7 billion), ECMS aims at developing India's electronics industry. This scheme focuses on increasing the domestic value addition in the electronics industry. This scheme currently aims to foster the production of electronic components such as multi-layer PCBs, camera modules, connectors, oscillators, optical transceivers, and enclosures for mobile and IT hardware products in the country. India's 2026-27 budget increased the total financial outlay for the ECMS to Rs. 40,000 crores, signalling the country's push for domestic electronics manufacturing (Press Information Bureau, 2026).

9.2.3 Production Linked Incentive (PLI) Scheme

The PLI scheme was launched in 2020 for mobile manufacturing and has expanded to 14 sectors such as mobile manufacturing, pharmaceuticals, textiles, electronics and IT hardware and advanced chemistry cell batteries. Till 2026, the program has had a combined budgetary outlay of Rs. 1.97 lakh crore (approximately USD 26 billion) allocated across various sectors. This PLI scheme offers financial incentives to companies based on their incremental sales, which in turn is expected to increase the manufacturing efficiency (Press Information Bureau, 2026).

9.2.4 Modified Electronics Manufacturing Clusters (EMC 2.0)

Launched in 2020, the EMC 2.0 scheme aims to create world-class infrastructure for electronics manufacturing by funding clusters with common facilities such as plug-and-play facilities, ready built factory sheds, etc. As of December 2025, 11 clusters have been approved under the scheme (Press Information Bureau, 2026).

10. India's Semiconductor Ambitions through the 3 pillar diagnostic

10.1 India and Technology

10.1.1 Weak Innovation and R&D ecosystem

India currently spends only 0.7% of its GDP on R&D while China spends 2.4% of its GDP and the USA spends 3.6% of its GDP. When combined with PPP adjusted GDP, this GERD spending translates into: China spends 2.4% of its USD 41.02 trillion PPP adjusted GDP and USA spends 3.6% of its USD 30.62 trillion PPP adjusted GDP, while India spends only 0.7% of its USD 17.71 trillion PPP adjusted GDP, showing how less India spends on its innovation capabilities (Silver, 2026).

A very similar case for corporate R&D intensity as well – Indian corporate companies have some of the lowest R&D spending in the world. Among the world's top 2000 corporate spenders on R&D, only 15 Indian firms – with a combined spending of USD 5.3 billion – were featured. The government contributes around 64% of the total GERD while the private sector covers around 34%. This is the opposite case in major countries like South Korea, Israel, USA, where the private sector contributes more than the government to R&D in terms of funding. Out of all the expenditures the top 500 companies in India incurred in the last decade, less than 1% went into R&D. And out of this meagre amount, a major share went into recurrent expenses such as wages, salaries, maintenance. A general tendency towards risk aversion and short-term gains is also another factor impeding private investment in R&D. Apart from these, India's universities publish very little world-class and market relevant research. This can be attributed to universities' struggle from the weak industry-academia linkage problem. India also faces the brain drain problem, where highly skilled scientists and engineers migrate to countries with better opportunities (Business Standard, 2023; NewsClick, 2026; Shivakumar & Sharma, 2025)

10.1.2 Skilled workforce shortage

According to the All India Survey on Higher Education 2021–2022, India has 36.6 lakh students enrolled in B.Tech and B.E courses, with about 8.25 lakh students awarded such degrees in FY 2021. However, a very small fraction of that number are industry ready, i.e., capable of working on the factory floor. Reports also show that most engineering students prefer getting data science or AI and ML courses and certifications, with very few interested in electrical and electronics engineering, which are key needs for semiconductor talent. Some reports also show that Indian graduates' exposure to semiconductor technologies is lesser than other technologies, and they choose the easier path to employability compared to semiconductor-hardware engineering. India is also expected to see a shortage of around 2.5 to 3 lakh semiconductor industry professionals by 2027, according to some estimates. This adds another layer of challenge for India's semiconductor industry ambitions. (Ezell, 2024a; Shivakumar & Sharma, 2026).

10.1.3 Competitive in Design segment

India currently has a considerable share in the Design segment of this industry. Out of the entire semiconductor design activity, around 7% of the activity happens in India and around 20%

of the professionals employed in this segment are Indians, with major firms such as Intel, Qualcomm, and AMD having Global Capability Centers (GCCs) in India.

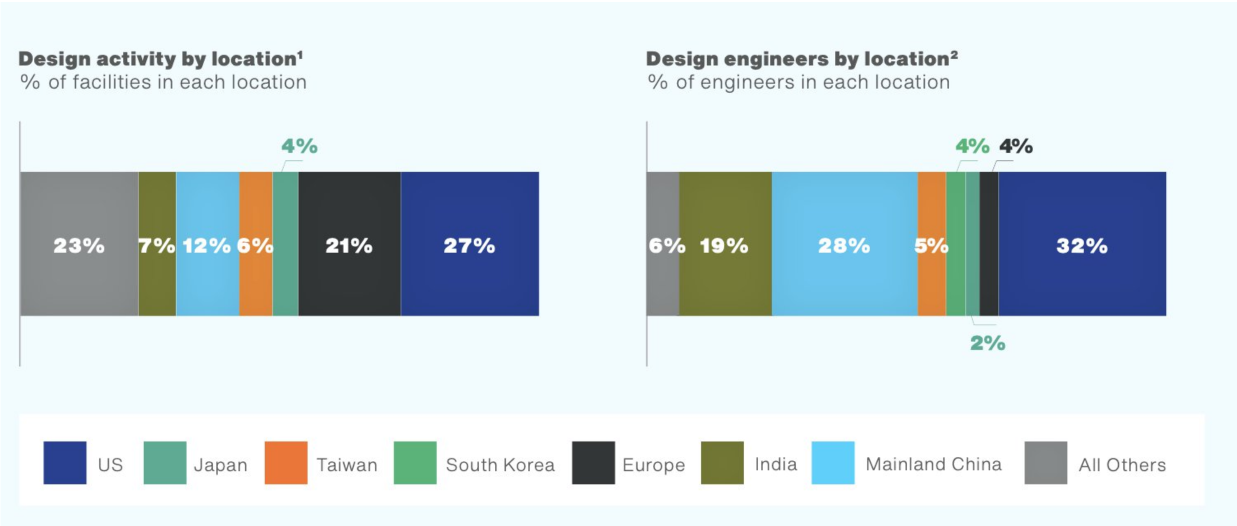

Figure 29 Design activity by location (% of facilities in each location) and Design engineers by location (% of engineers in each location)

(Source: BCG Analysis)

10.2 India and Industry

10.2.1 Infrastructure bottlenecks

India's electricity supply reliability has been questioned often. But, semiconductor fabs and OSAT facilities need uninterrupted power supply. High costs of electricity for industries also make manufacturing in India some of the costliest in the world. The 2025 Economic Survey says that the higher cost of electricity for industrial purposes is one of the major factors impeding the country's manufacturing sector. This is in stark contrast to the lower prices paid by households (Times of India, 2025). This points at how the "cross-subsidization" phenomenon is silently harming industrial activity in the country. More than the electricity costs, it is the energy mix of the country and the different states that needs focus. More than 75% of the electricity produced in the country still comes from non-renewable sources such as coal and oil, which are polluting in nature (NITI Aayog, 2023).

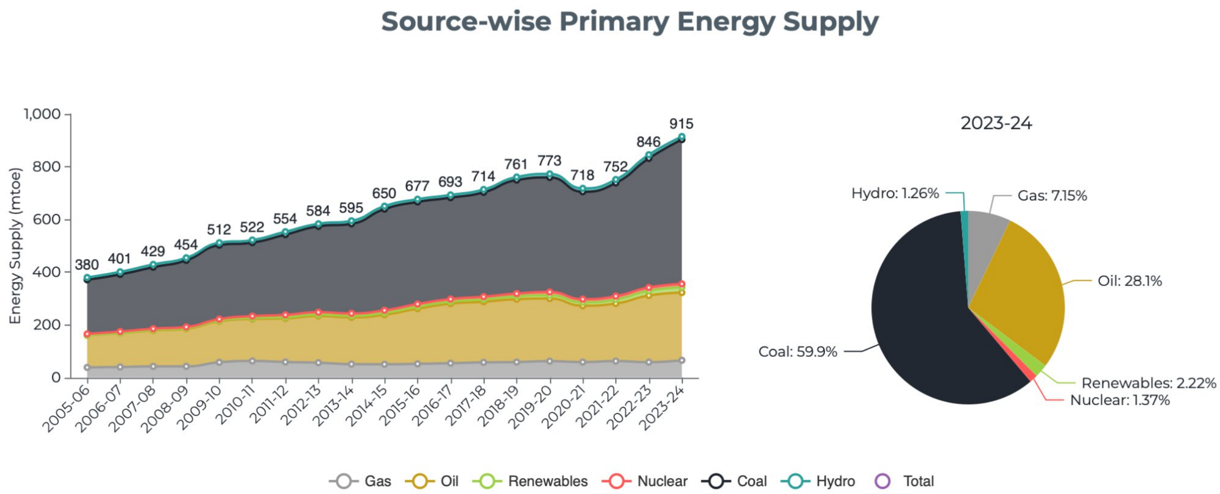

Figure 30 India's source-wise primary energy supply

(Source: Ministry of Power)

These fabs also use huge amounts of water. Given India's declining groundwater table, drying up rivers and changing rain patterns due to climate change, it is a question as to whether India will be able to sustain the industry's high water requirements. Fabs are huge in terms of their size and need large land parcels. India's complicated land ownership patterns, along with the high number of legal issues involved in land ownership again act as a structural bottleneck. India's transport and logistics infrastructure is improving, but other countries are edging in this aspect as well. For instance, a study says that a 2000 km delivery can be done in 24 hours in China while it might take 5 to 7 days in India. India has increased the number of airports (from 74 to 141) and rail network connectivity considerably in the last few years (Ezell, 2024a).

10.2.2 Weak electronics manufacturing base

India has emerged as a leading hub for electronics assembly in the last decade, especially for smartphones and consumer electronics. The domestic value-addition in these segments are as low as 15-20%, since the major components such as displays, batteries, camera modules are still imported. Although the domestic production of electronic goods increased from INR 1.90 lakh crore in FY 2014-15 to INR 9.52 lakh crore in FY 2023-24, and the exports of electronic goods increased from INR 0.38 lakh crore in FY 2014-15 to INR 2.41 lakh crore in FY 2023-24, India's imports of key components from China, South Korea and Japan have remained high. And importantly, most of this growth in production and exports happened in the smartphones segment. One of the key reasons for India's electronics industry still in the low-value assembly segment is the lack of technology for producing the key components (Singal, 2025).

10.3 India and Geopolitics

10.3.1 Bilateral Engagements

India has made significant progress in building the diplomatic foundation for semiconductor cooperation. One of them is the Tata-PSMC agreement, where PSMC provides design, construction and engineering support to the fab being set up in Gujarat, licensing a number of technologies, and training hundreds of Tata employees in equipment handling, process technology, and quality engineering. The IMEC research organization and India have a tech transfer agreement where IMEC will transfer the technology to manufacture 28nm and above chips. India has signed a Memorandum of Understanding with Singapore to establish the India-Singapore Semiconductor Ecosystem Partnership, and a Memorandum of Cooperation with Japan to develop a resilient semiconductor supply chain. (DD News, 2025; Electronics For You, 2024; Singh, 2023)

10.3.2 India's engagement with the USA

At the multilateral level, India has joined several US-led initiatives. India and USA have established the TRUST (Transforming the Relationship Utilizing Strategic Technology) initiative replacing the iCET (Initiative on Critical and Emerging Technologies) to improve bilateral cooperation in AI, semiconductors, defence and space. India has also signed agreements with the USA as part of USA's International Technology Security and Innovation (ITSI) Fund to secure the semiconductor supply chains. Apart from these, the Quad Alliance, which includes India, the USA, Australia and Japan has a focus on securing and strengthening the semiconductor supply chains. India has also joined the Pax Silica, a US led initiative to secure and strengthen the global supply chains for AI, semiconductors and critical minerals. India is also part of the Indo Pacific Economic Framework, a US-led initiative aimed to strengthen the economic cooperation among 14 Indo-Pacific countries in the 4 pillars of engagement: Trade, Supply Chains, Fair Economy and Clean Economy (India's World, 2026; Office of the Principal Scientific Adviser, 2025; U.S. Department of Commerce, n.d.; Wise & Ezell, 2022)

10.3.3 Assessment of these initiatives

The critical question is not how many agreements India has signed, but what those agreements actually deliver in terms of technology depth and alliance trust. While TSMC is setting up new fabs in the USA and Japan, it declined India's invitations to set up fabs in India. Similarly, the now rescinded US AI Diffusion Rule placed India in Tier 2 list of countries, capping its access to high-performance chips, while Tier 1 countries including South Korea, Japan, the Netherlands and Taiwan enjoy seamless access (The Hindu, 2025; The Economic Times, 2025). These examples mirror the 3 pillar framework described above: countries receive the technology their geopolitical standing and industrial ecosystem entitles them to, not necessarily the technology they need to move up the value chain.

India’s relationship with Russia and Iran are the most challenging points in the India-USA relationship. India has deepened its energy and trade relationship with Russia since 2022, and has emerged as a significant supplier of dual-use technologies to Russia. The US Foreign Direct Product Rule, which mandates allies to restrict exports of products developed using US technology to restricted countries, is directly relevant here (Lee & Nellis, 2022; The Hindu BusinessLine, 2025). If India and the US deepen their technology sharing arrangements, Washington will inevitably ask whether India will comply with such export control demands – and India's historic relationship with Russia creates genuine doubt on that front.

The broader geopolitical context makes India's position both more valuable and more precarious simultaneously. China’s aggression against the USA both directly and indirectly – in terms of trade wars, competition in the technological space, placing restrictions on rare earth minerals, etc. is increasing. China’s aggressive behaviour towards countries like Taiwan and Philippines (which are under US security support) has also increased. These combined with the China-Russia-North Korea nexus in Asia has made the US’ need to build trusted alternatives in the Indo-Pacific more eminent than ever. In this context, India is geopolitically significant for the US in South Asia. India’s neighbourhood signifies this: Pakistan, Bangladesh, Maldives and Sri Lanka have a soft relationship with China, making India the only credible anchor who has the adequate technological and industrial capabilities in the South Asian region, for the USA.

Yet, a stronghold in South Asia does not automatically translate into priority in semiconductor strategy. The US and its allies are first working to loosen the Taiwan chokepoint by deepening investments in Japan and South Korea which have decades of semiconductor experience and have been long standing alliance partners. The EU is also emerging as a geographically closer destination to the USA, aimed at reducing the overall concentration in the

East Asia region. TSMC building fabs in USA, Japan and Germany, while declining India's invitations, reflect this hierarchy. Although the "China plus One" rhetoric has taken shape, China's dominance in legacy chips and its ongoing efforts to increase its production capacities means a complete decoupling from China is not imminent. And the West's strategy is likely to be gradual diversification and shifting the conflict zones away from the Pacific and not sudden reshoring. In that gradual process, India must compete with Vietnam and other Southeast Asian nations who have made significant gains in the China plus One era.

The window for India is real, but narrow and conditional. It will remain open as long as the US-China rivalry intensifies and India remains the most viable Indo-Pacific partner outside of East Asia. What India does within that window to strengthen its technology transfer arrangements, and build the technological and industrial base that makes it genuinely valuable rather than merely convenient, will make the discourse not merely geopolitical, but geoeconomical as well. And this will determine whether India secures a strategic position in the global semiconductor supply chain or remains a peripheral node in it.

11. Policy Recommendations: Building a Sustainable Semiconductor Ecosystem in India

11.1 India needs a Techno-Industrial Policy and Mission-driven innovation

India should adopt a techno-industrial policy approach that integrates industrial expansion with technological development and developing indigenous innovation capabilities. Fostering innovation in critical technologies such as AI, semiconductor technologies, quantum computing and space technologies should be done on a mission-mode, mandating the coordinated efforts of the government, industry, and research institutions.

Taking into consideration the strengths and weaknesses in India's technological capabilities, industrial capabilities and geopolitical environment, India's semiconductor strategy needs to adopt a short-term, medium-term and long-term approach.

11.1.1 Short-Term Plan (0-5 Years)

11.1.1.1 Prioritize ATMP, strengthen Design and selective Fabrication entry

India should prioritize assembly, testing, marking, and packaging as an entry point, since this segment offers relatively lower entry barriers while still giving an entry point into global supply chains. At the same time, India should strengthen its design services, which provides a stronger integration into the global value chain and thus complements India's movement into fabs. Due to the high capital intensity and technological complexity, immediate large-scale investments in fabs may not yield sustainable outcomes without supporting capabilities and industries. Thus, they should be selectively and strategically pursued, aligned with domestic demand and ecosystem readiness

11.1.1.2 Leverage foreign technology while building absorptive capacity

Technology transfer will be critical in the early stages, as seen in the Tata-PSMC example. India should actively attract global semiconductor firms and skilled professionals to establish and operate facilities domestically. At the same time, emphasis must be placed on building absorptive capacity – training Indian engineers and technicians to learn, adapt and improve upon imported technologies. India should make use of its present geopolitical alliances and partnerships, such as the Pax Silica, Quad, TRUST, to bring in the latest technologies and personnel for this purpose. With a large diaspora in the USA and EU, India can bring back engineers and professors having industry exposure and hands-on experience to design industry relevant courses and upskill the Indian workforce.

11.1.1.3 Develop semiconductor clusters linked to existing industrial ecosystems

Semiconductor facilities should be located within or near established electronics manufacturing clusters. Establishing dedicated Semiconductor Clusters with dedicated facilities, utilities and logistics infrastructure can further enhance the competitiveness of the cluster.

11.1.1.4 Invest in foundational STEM education and workforce training

The government should invest in foundational STEM education and specialized semiconductor training programs. In addition, India can leverage the global skill shortages by encouraging the temporary migration of engineers to leading semiconductor countries for gaining hands-on experience.

11.1.2 Medium-Term (5-10 Years)

11.1.2.1 Expand the domestic electronics and manufacturing base

A strong semiconductor ecosystem requires robust downstream industries. India must accelerate the growth of its electronics, automotive, telecommunications, and defence manufacturing sectors, and ensure their consumption of chips manufactured in India.

11.1.2.2 R&D ecosystem reforms

India’s weak industry-academia linkage issue needs to be addressed. Policies should incentivize collaborative R&D between industry and researchers/students via industry-funded university projects ensuring applied research caters to market needs. The government should create enabling conditions (such as strong intellectual property protection) that encourage private firms to invest more in applied and frontier R&D.

11.1.3 Long-Term (10-20 Years)

11.1.3.1 Align fabrication expansion with ecosystem maturity

Depending on the development of a strong industrial base, skilled workforce, and supplier ecosystem, further expansion of fabrication capacity should be done. Fabs should be embedded within a broader industrial ecosystem that is capable of sustaining high productivity, efficiency and continuous process innovation.

11.1.3.2 Build capabilities in high-value upstream segments

India should invest in developing upstream segments such as semiconductor manufacturing equipment, materials, and process technologies. These segments capture higher value and offer strategic leverage but require sustained investment in precision engineering, materials science, and advanced manufacturing.

Limitations

Several limitations of this study need to be acknowledged. First, relying exclusively on secondary sources means the analysis is bounded by the quality, recency, and credibility of publicly available documents. Second, the three-pillar framework, while analytically useful, is a simplification. In practice, the boundaries between technology, industry, and geopolitics are fluid and closely interlinked in ways that a triangulated structure cannot fully capture.

Future Scope of Research

This study opens several avenues for future research. First, primary research including structured interviews with policymakers, industry leaders, and researchers within India's emerging semiconductor ecosystem would substantially deepen the analysis and provide ground-level perspectives that secondary research cannot capture. Second, as India's fab projects move from construction to production, studies to track actual learning-by-doing outcomes, yield rates, and knowledge spillovers would provide empirical results for the claims made here about industrial learning. Third, a more granular examination of the depth and conditionality of India's technology transfer agreements, particularly the Tata-PSMC deal and the various US-India frameworks, would help assess whether India is receiving technology that genuinely enables India to move up the value chain or merely improve its production capacity.

Conclusion

The global semiconductors race is not merely a technological race, but is a convergence of countries' technological capability, industrial depth, and geopolitical positioning. This study has argued that these three forces are not independent but together form a mutually reinforcing system, and understanding their interaction is essential for any country seeking to build a sustainable semiconductor strategy. The historical trajectories of Japan, South Korea, Taiwan, and China confirm this understanding. Each of these countries succeeded through a long-term alignment of state strategy, industrial development, and geopolitical access to frontier knowledge.

Applied to India, this framework reveals a country at a critical inflection point. India has the right ambitions, a growing policy architecture, and a genuine geopolitical window created by the vulnerabilities in today's world. But ambition and opportunity alone are insufficient. The three-pillar diagnostic reveals that India's technology pillar is constrained by low R&D spending, weak industry-academia linkages, and a predicted workforce shortage. Its industry pillar is limited by a thin electronics manufacturing base characterized by low domestic value addition, and persistent infrastructure bottlenecks. And its geopolitics pillar, while diplomatically active, is undermined by the shallow depth of technology transfer the country is receiving and the credibility gap rooted in its tradition of strategic autonomy and non-alignment.

The sequenced policy recommendations in this study offer a realistic pathway forward. India does not need to replicate the strategies of Taiwan, Japan or South Korea. It needs to find its own segment-specific position in a global value chain that is dynamically being restructured by geopolitical forces, and strategically enter these segments in a manner that is aligned with its existing industrial capabilities, geopolitical relationships, and long-term technology ambitions, before the window of restructuring closes. The countries that act decisively in this period of flux will be the ones that define the future of semiconductor competitiveness.

The semiconductor industry rewards those who build patiently, invest consistently, and position strategically. India has the pieces to the puzzle. Whether it has the resolve to assemble them in time will determine whether it secures a strong and resilient position in the global semiconductor supply chain or remains a peripheral node in it.

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